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PROJECT ADMINISTRATION DATA SHEET

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oject No. E-21-683 GTRI/~~GIT~~ DATE 6 / 21 / 84

oject Director: J. P. Uyemura ~~School~~/Lab Elect. Engr.

onsor: IBM Corporation

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	This Change	Total to Date
Estimated:	$ 56,186	$ 56,186
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le: Physical Limitations on Bipolar Digital Integrated Circuits

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Physical Limitations

tive Completion Date: 9/15/84 (Performance) 9/30/84 (Reports)

/Contract Closeout Actions Remaining:

- [ ] None
- [X] Final Invoice or Final Fiscal Report
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Physical Limitations on Bipolar Digital Integrated Circuits

Progress Report

5 January 1984

John P. Uyemura
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332

The basic objective of this research has been to examine the formation of the noise margins (NM) in ECL bipolar integrated circuits. The problem of minimum power supply levels has been included in a complimentary manner. This report will summarize the work performed thus far, with emphasis upon the results and their implications in an overall sense. It will also detail the plan for the next phase of the research project.

The work on the problem has progressed along the lines presented in the original proposal. In particular, the studies up to this point have centered around three primary areas, namely, (a) a study of the basic features of the IBM bipolar fabrication process as discussed in the open literature; (b) the initial analysis of the problem of interconnect coupling; and (c) the noise margin formation in a basic 2-Input OR/NOR ECL gate. The examination of the IBM bipolar processing was included only to obtain a basis for the analysis, and will not be discussed in detail here.

The problem of interconnect signal coupling as an interference (noise) source in the integrated configuration has been studied using standard transmission line analysis. A lossless transmission system has been assumed for simplicity, but it is felt that the analysis can be extended to include the effects of sheet resistances in a relatively straightforward manner. The basic model consists of two interconnect (metal) layers which are taken in a rectangular grid arrangement. The coupling between interconnect layers has been modelled as being purely capacitive, as this allows for the simplest analysis; fringing field corrections are included in the model.

The signal dynamics of the model is obtained by assuming that a step-like voltage transition of the form u(t) or [1-u(t)] is propagating on one of the lines. This then approximates the case where a circuit undergoes a switching event, and the interconnect is transmitting the signal to the next logic stage. The coupling problem arises when a portion of the signal energy is induced onto a neighboring line, which in turn feeds the input of an arbitrary gate in the logic array. This situation is particularly important to the study of input transition widths in the ECL circuit, since the coupling may lead to false interpretation of the logic levels.

The basic problem has been cast into the study of coupling parameters as functions of the basic processing variables. For example, the metal-to-metal oxide thickness is left as a variable in the analysis, which then allows for quantitative trends to be established for specific cases. The ground rule spacings are also included to insure that the analysis can be varied according to the technology constraints. This has lead to the derivation of some basic design constraints in the form of transmitted voltage equations. In their generalized form, the equations demonstrate the frequency-dependent coupling as a function of certain key processing parameters in the chip structure. Although this type of coupling is not expected to be significant at the gate level, it is thought at this time that it will play a role in determining the overall chip noise margin, since the off-chip drivers may lead to significant back-coupling. Owing to this observation, further studies on this type of coupling mechanism are being discontinued until the off-chip drivers are analyzed. The problem will then be reintroduced in the context of overall chip layout guidelines.

The majority of the work performed thus far centers around the noise margin formation in a simplified 2-Input ECL OR/NOR gate; Schottky-clamping is used at the inputs to insure that the analysis remains in the non-saturated regions. The initial studies dealt with the hand analysis of the switching properties of the circuit, with emphasis upon both the device modelling and the circuit design for the noise margin levels. The simplified Ebers-Moll equations proved sufficient to understand some of the more basic properties, but were

unable to adequately account for the device physics. Consequently, the Ebers-Moll reverse saturation currents were modified to allow for Gummel number variations in the processing. A full charge-control analysis is also in progress, which allows for the inclusion of factors such as depletion charge variations.

The analysis is directed towards obtaining equations which are capable of demonstrating the most important parameters for setting the noise margin in the circuit. The input transition widths are also being studied for Fan-in and Fan-out considerations. Sensitivity factors are very important in these calculations, as they allow for the explicit variations in the noise margins to be plotted as functions of the different parameters. The results have been along the expected lines, with factors such as operating temperature and bias current/voltage levels being of prime importance. The low-voltage possibilities of the circuit configuration have also started to appear, since the analytic expressions automatically contain the power supply levels. In addition, two factors have been found to be crucially important, namely, the actual Gummel number of the base doping profile and the exact shape of the transistor transfer characteristics. Although these dependences were expected before the analysis was performed, their importance in establishing the overall voltage transfer curves of the circuit were greater than anticipated. The modelling will be taken one level deeper in the next few months by including some of the more important device properties of the integrated transistor layouts. In particular, work is already underway to examine the effects of an ion-implanted emitter region in terms of the Gummel number variations of a transistor.

The analysis described above is being complimented by computer circuit simulations using the SPICE II CAD program. The basic device modelling provided in SPICE has allowed for a correlation of the simulated circuit responses with the analysis. It also provides for a straightforward approach to testing some of the more important parametric dependences, e.g., the NM dependence upon temperature variations. At the current time, the correlation is being performed in a "brute-force" manner by varying circuit and device parameters from run-to-run. The results are being tabulated to extract the

important factors which contribute to the noise-margin formation problem. Although Fan-in and Fan-out values of unity were assumed in the initial tests, these have been expanded to more realistic numbers. Voltage supply values range from about 1.0 V to 2.0 V, with emphasis upon computing the values of the transition widths, the logic (output) swings, and the noise margins.

The studies have started to result in some interesting properties of the 2-Input OR/NOR circuit, which are being expanded to multiple-input gate configurations. Items such as the relative insensitivity of the noise margin to transistor β variations have allowed for greater simplifications to be made in the analysis. In addition, the circuit simulations are setting the stage for specifying a set of optimum design criteria for maximum noise immunity values. Since the current data is not yet sufficient to finalize these trends, a detailed discussion of the results will not be presented here.

The program will continue in the same directions as described above. During the next phase of research, emphasis will be placed upon finding the most important parameters needed for the correlation between the device/chip physics and the noise margin levels in the ECL configuration. It is felt that this will require further circuit simulations with improved device modelling. Also, some of the overall chip structuring problems will be introduced into the overall analysis. This includes items such as the off-chip driver circuits.

E-21-683

GEORGIA INSTITUTE OF TECHNOLOGY
SCHOOL OF ELECTRICAL ENGINEERING
ATLANTA, GEORGIA 30332

PHONE: (404) 894-2961

July 11, 1984

Mr. D. B. Mooney, D/29A, Zip 47A
IBM General Technology Division
East Fishkill Facility, Route 52
Hopewell Junction, New York 12533

SUBJECT: Quarterly Report, IBM Purchase Order No. 7S-785515, Project Director - J. P. Uyemura, Project Entitled, "Physical Limitations on Bipolar Digital Integrated Circuits", Period of Performance - 1/1/84 - 6/30/84

Dear Mr. Mooney:

Enclosed is the quarterly report for the subject IBM purchase order. The period covered by this report is January 1, 1984 - June 30, 1984.

If you have any questions or comments concerning this report, please contact Dr. John P. Uyemura at (404) 894-2975.

Thank you.

Sincerely,

Marsha Segraves
Admin. Asst.

cc: J. P. Uyemura
OCA (2)

/ms

PHYSICAL LIMITATIONS on
BIPOLAR DIGITAL INTEGRATED CIRCUITS

John P. Uyemura
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, GA 30332

PROGRESS REPORT

1 January 1984

to

30 June 1984

The overall objective of this research project has been to examine to problem of Noise Margin (NM) formation in bipolar digital integrated circuits, with emphasis towards Emitter Coupled Logic (ECL). A simultaneous problem under investigation has centered around the minimum power supply voltage level which may be employed in the circuits while maintaining acceptable switching levels in the system. This Progress Report will present the details of the results obtained over this time period, and will summarize the plan for the remaining portions of the work.

In order to present the work in a coherent manner, the discussion will be divided into sections. Each section will detail a specific aspect of the research, and will be concerned with the presentation of details of the problem under study. Owing to the desire to keep the report relatively concise, only results will be stated. The intermediate analysis will be reserved for the Final Report.

1. Interconnect Coupling

As was mentioned in the Progress Report of 5 January 1984, a substantial amount of effort has been directed towards analyzing the problem of unwanted coupling between stages via parasitic capacitances. The analysis has been initially centered around the simplified dual-interconnect model illustrated in Fig. 1(a). Here it is seen that the chip structure in the region of interest has two distinct levels of interconnect materials. The switching circuits are denoted as

Stage 1 and Stage 2, respectively.

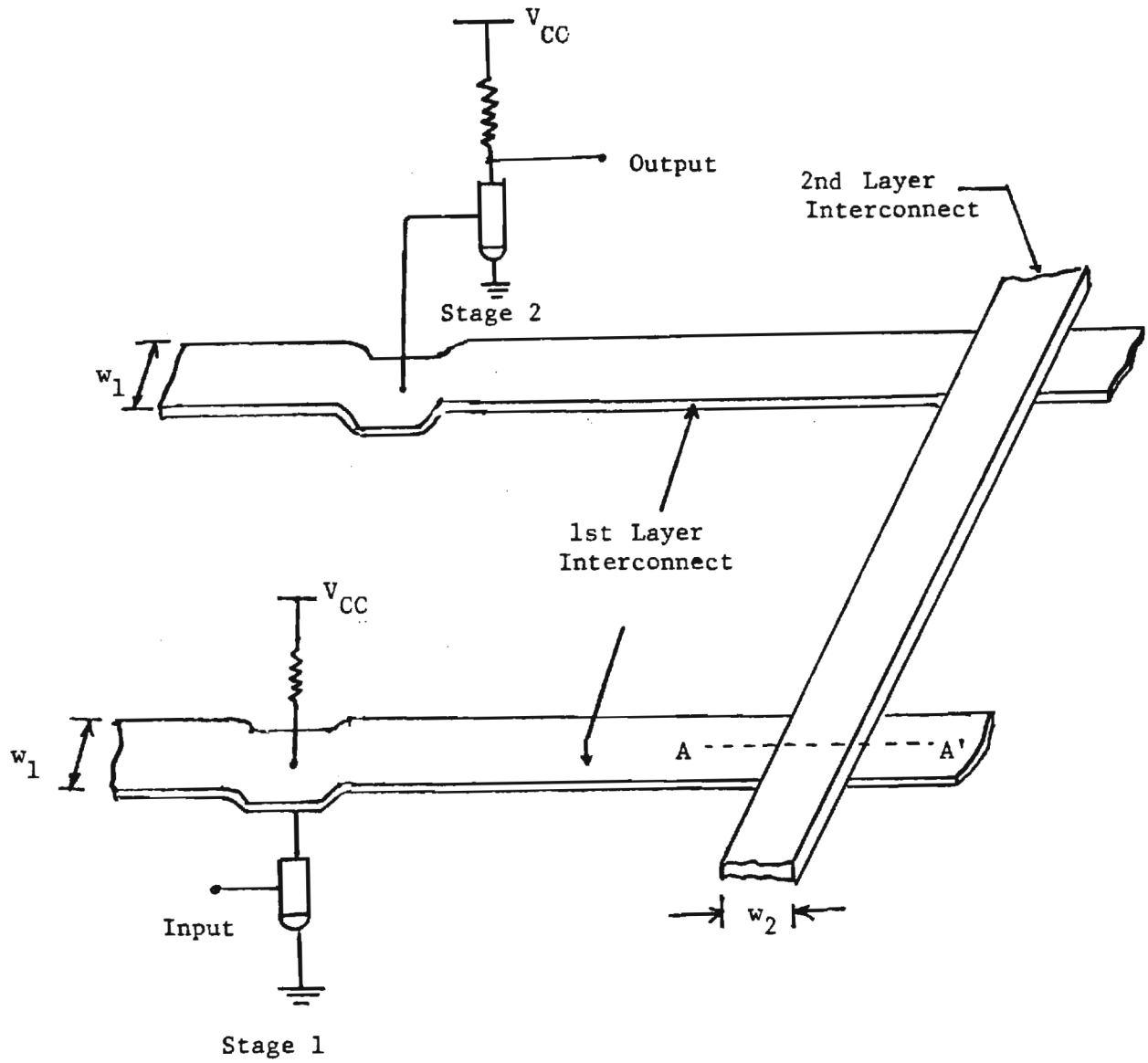
The basic problem under consideration here deals with the case where the circuitry in Stage 1 undergoes a switching event. The voltage wave then propagates to the right (towards the next stage in the logic), but is coupled onto the 2nd layer interconnect line by capacitive means. Although Stage 2 is not directly driven by any logic during this transition, it is seen that induced interference back down to the 1st level of interconnect may create a false switching event.

The illustration in Fig. 1(b) shows the assumed cross-sectional view of the interconnect layers. In terms of the separations d_1, d_2 and $d=d_1+d_2$, the system oxide capacitances per unit area may be estimated as

$$C_1 = \frac{\varepsilon_{ox}}{d_1} \quad , \quad C_2 = \frac{\varepsilon_{ox}}{d_2} \quad , \quad C = \frac{\varepsilon_{ox}}{d} \qquad [F/cm^2] \qquad (1)$$

where ε_{ox} represents the oxide permittivity. This ignores the presence of any fringing fields, and also assumes that the insulating oxide is homogeneous.

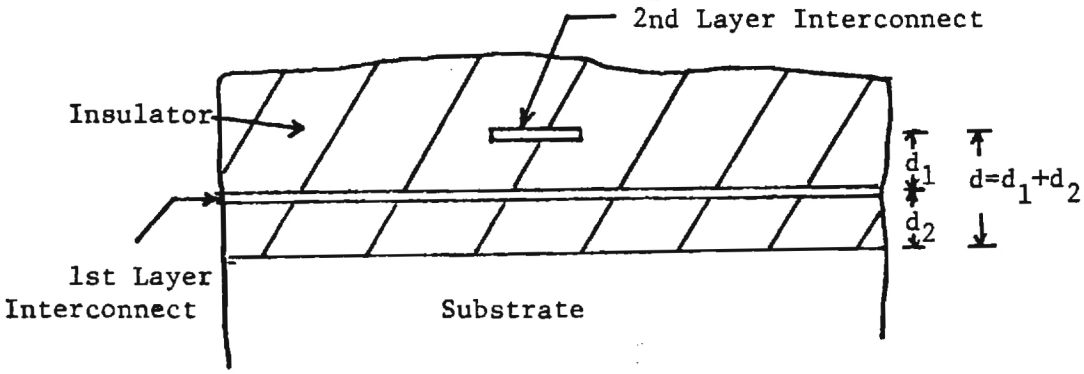
In order to simulate the basic coupling problem, the interconnect structure is modelled as the transmission line arrangement illustrated in Fig. 1(c). The characteristic impedances of the lines are denoted by Z_1 and Z_2, which respectively describe the 1st and 2nd layer interconnect levels. Owing to the fact that wavelength effects may become important in the transmission structures, the line lengths ℓ_1, ℓ_2 and ℓ_3 have been introduced.



Simplified Model for
Coupling Problem

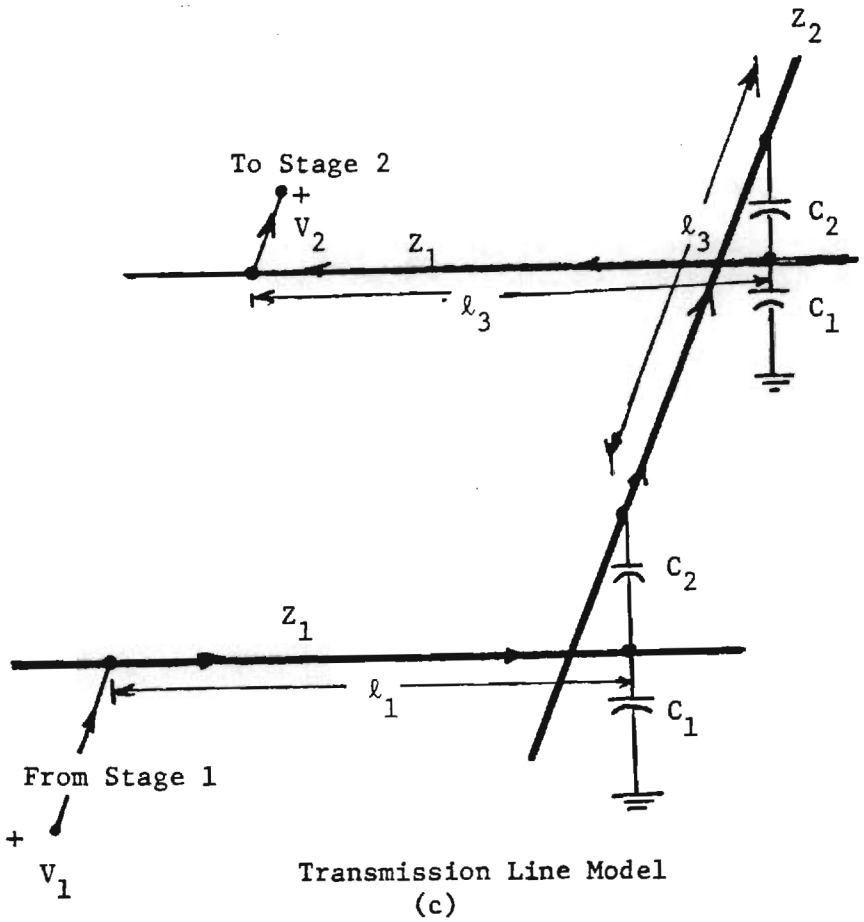
(a)

Figure 1



Cross-Sectional View along AA'

(b)



Transmission Line Model

(c)

Figure 1

Interconnect Coupling Problem

The solution to the coupling problem is relatively straightforward in nature. The intial wave front is established on the 1st layer interconnect with length ℓ_1. The wave then propagates to the right, where it is coupled onto the 2nd layer line with length ℓ_2. The signal then propagates along the path shown in Fig. 1(c), where it is then coupled back to the 1st layer interconnect line which feeds the input of Stage 2. The basic voltage waveforms of interest are V_1 and V_2. Note that each coupling point induced waves travelling in both possible directions.

The easiest case to consider is that where the wavelength λ of the wave satisfies

$$\lambda >> \ell_1, \ell_2, \ell_3 \quad . \tag{2}$$

In the frequency domain analysis, this allows for the derivation of a transfer function $H(j\omega) = (V_2/V_1)$ of the form

$$H(j\omega) = \frac{C_2}{C_2 + 2C_1} = \frac{d_1}{d_1 + 2d_2} \quad . \tag{3}$$

which is a constant. This, of course, corresponds to the simplistic model where the propagation is ignored, and the signals are modelled by means of a lumped equivalent circuit.

A more realistic case is that where the voltage wavefront is decomposed into a series of time-harmonic functions, but where the wave nature of each frequency component is accounted for in the analysis. This has been examined by employing the concept of lumped-equivalent

impedances at the coupling points, while maintaining the length-dependent impedance properties of the transmission lines themselves. Losses (i.e., resistance) in the lines have been ignored for simplicity. It has been found that the transfer properties can be described by means of the input impedance Z_{in} as seen from the Stage 1 entry point to the Stage 2 exit point. The analysis gives

$$Z_{in} = Z_1 \frac{[Z_{C1}||Z_1||Z_X] + jZ_1\tan(\beta\ell_1)}{Z_1 + j[Z_{C1}||Z_1||Z_X]\tan(\beta\ell_1)} \tag{4}$$

where "||" indicates parallel impedance connections,

$$Z_X = Z_{C2} + Z_2||[Z_2 \frac{Z_Z + jZ_2\tan(\beta\ell_2)}{Z_2 + jZ_Z\tan(\beta\ell_2)}] \tag{5}$$

and

$$Z_Z = Z_2||[Z_{C2} + Z_1||Z_{C2}||(Z_1 \frac{Z_L + jZ_1\tan(\beta\ell_3)}{Z_1 + jZ_L\tan(\beta\ell_3)}) \quad . \tag{6}$$

Z_L represents the "load impedance", which is the input value seen at the base of the transistor in Stage 2. Z_{C1} and Z_{C2} are the usual lumped equivalent values

$$Z_{C1} = -\frac{j}{\omega C_1} \quad , \qquad Z_{C2} = -\frac{j}{\omega C_2} \tag{7}$$

with ω the frequency and $\beta = (2\pi/\lambda)$ the wavenumber.

Although these results appear somewhat complicated, they may be understood by tracing the couplings point-by-point. They are well suited for a computer simulation, which is now in progress. This

requires that a Fourier resolution be performed in order to obtain the frequency components of the exciting (e.g., V_1) wave front for the system. The use of a computer simulation also allows for the study of a more complicated 2-dimensional grid structure, as shown in Fig. 2 on the next page. This problem is concerned with the estimating the "effective coupling length" L which is defined to be the maximum distance from the source (the switching stage) over which significant interference occurs. Thus, if L is known, it may be used to estimate the surface area which is subject to false switching. This work is being performed with the aid of an IBM PC, which allows for interactive programming variations.

Some obvious results may be stated at this point in the research. First, the complete lumped-equivalent modelling gives rise to the transfer function in eqn. (3). This may be used to state that the least amount of interconnect coupling will occur when the 2nd level distance d_2 is large compared to the 1st level spacing d_1. If $d_1=d_2$, H = (1/3), while setting $d_2=2d_1$ gives H=(1/6). This ratio, of course, is set by the fabrication process flow. It is important to note that this simplified analysis indicates that the interconnect separation distances may be scaled without affecting the coupling process. This means that if the separations are reduced to d_1/S and d_2/S with S>1 a scaling factor, then H is invariant.

Another effect which can be deduced is that the interconnect lengths become important. This is particularly true for transmission of the higher-order harmonics which contribute to the "squareness" of the switching waveform. Although the function Z_{in} is frequency-dependent, it appears possible to minimize the coupling by judicious layout procedures.

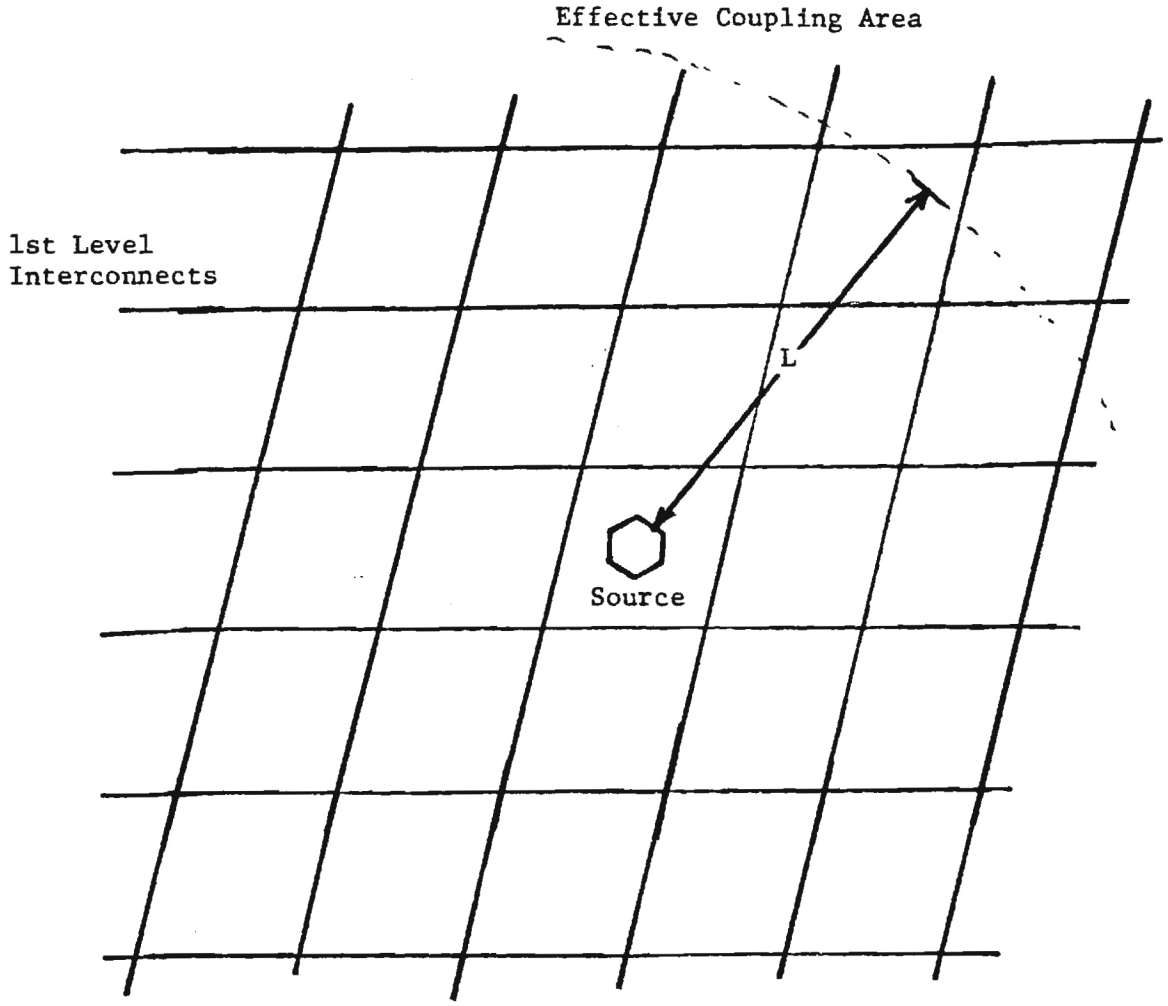


Figure 2

Grid Structure for Coupling Calculation

2. Switching Characteristics for ECL

This portion of the research has been directed toward an examination of the basic switching properties of a simplified 2-Input OR/NOR ECL circuit using the SPICE circuit simulator. The basic circuit is shown in Fig. 3 on the following page, and was modelled after the standard ECL 10K series of SSI. The primary objective of this study has been to subject the basic circuit to variations in device and operating parameters in an effort to extract the switching characteristics of importance. The voltage quantities which have been analyzed are denoted as

V_{OH} = Output High Voltage
V_{OL} = Output Low Voltage
V_{IH} = Input High Voltage
V_{IL} = Input Low Voltage

where "high" and "low" refer to equivalent Boolean "1" and "0" states. The Noise Margins of central importance are then taken to be

$$NMH = V_{OH} - V_{IH} > 0$$
$$NHL = V_{IL} - V_{OL} > 0 \quad .$$

The parametric variations have been summarized by a series of graphs which represent various circuit changes. As an example, consider the set of graphs contained in Fig. 4. These represent the variations in the important quantities as functions of the transistor common-emitter gain β_F. The three graphs show the variations at three different temperatures, and show that the circuit performance is not a strong

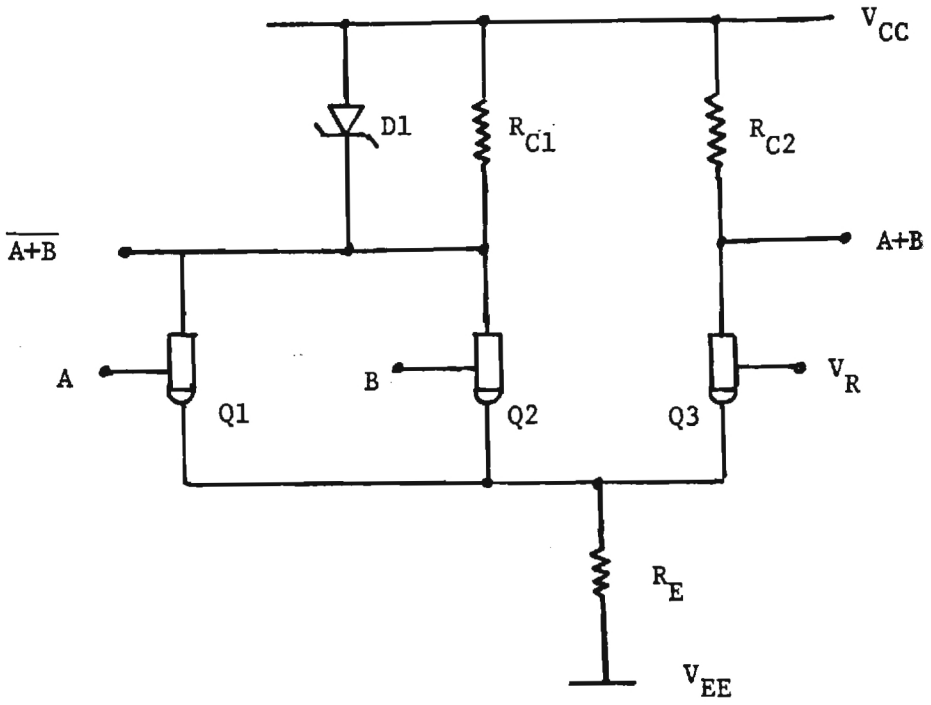


Figure 3

Basic ECL 2-Input OR/NOR Circuit

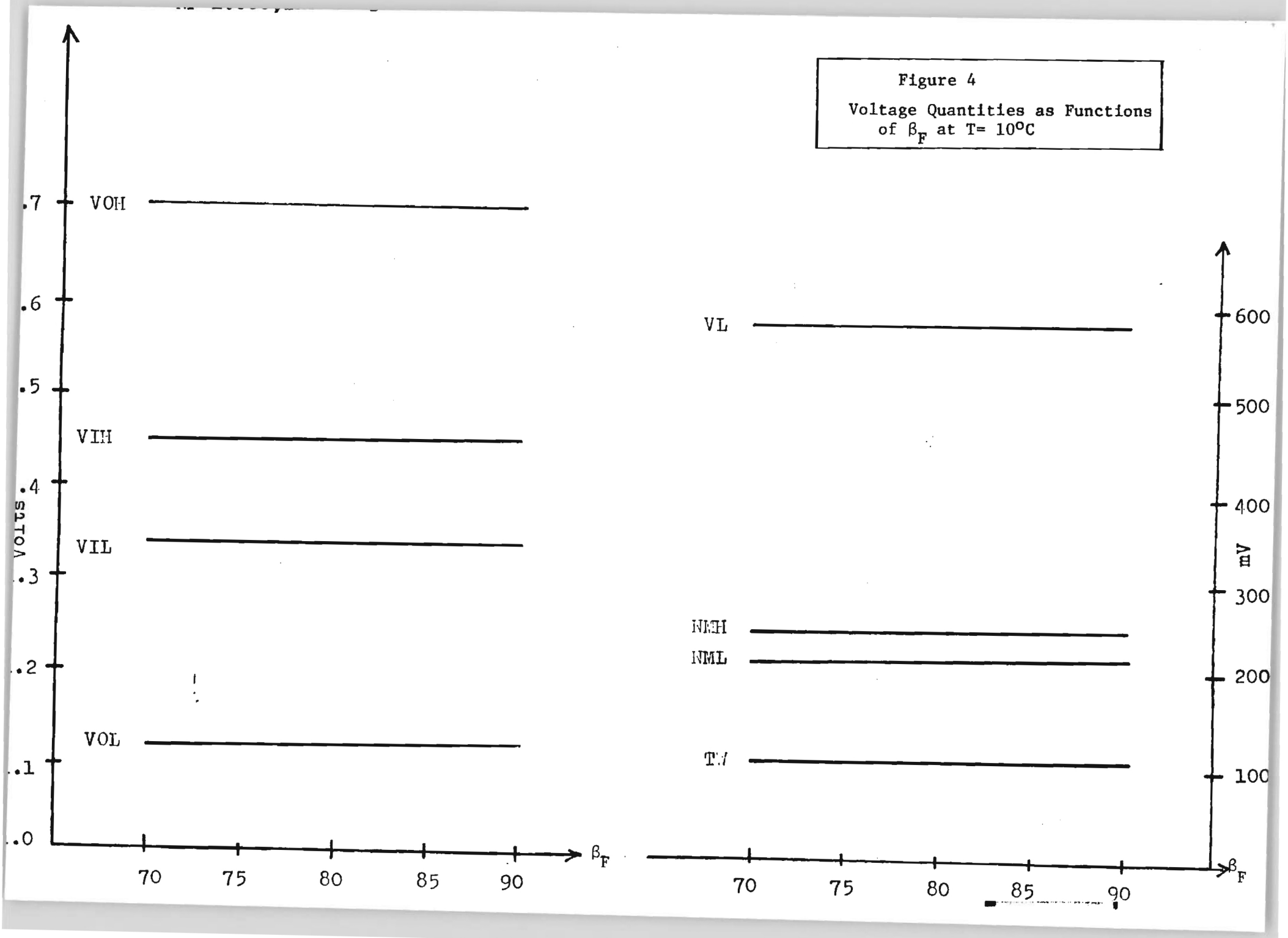


Figure 4
Voltage Quantities as Functions of β_F at T= 10°C
.7
.6
.5
.4
.3
.2
.1
.0
Volts
VOH
VIH
VIL
VOL
70
75
80
85
90
β_F
VL
NMH
NML
600
500
400
300
200
100
mV

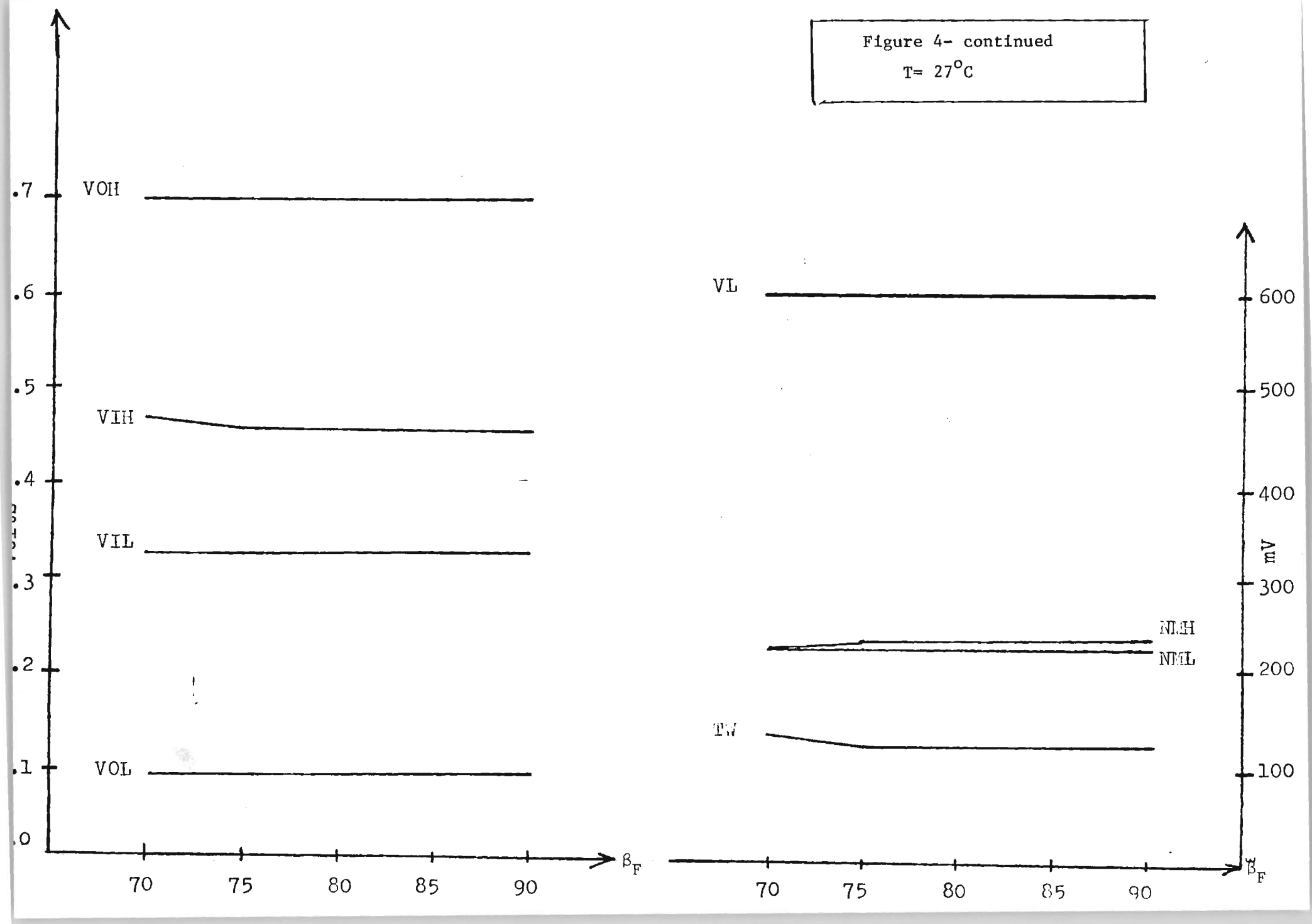


Figure 4- continued
T= 27°C
.7
.6
.5
.4
.3
.2
.1
.0
VOH
VIH
VIL
VOL
70
75
80
85
90
β_F
VL
NIH
NIL
TW
600
500
400
300
200
100
mV

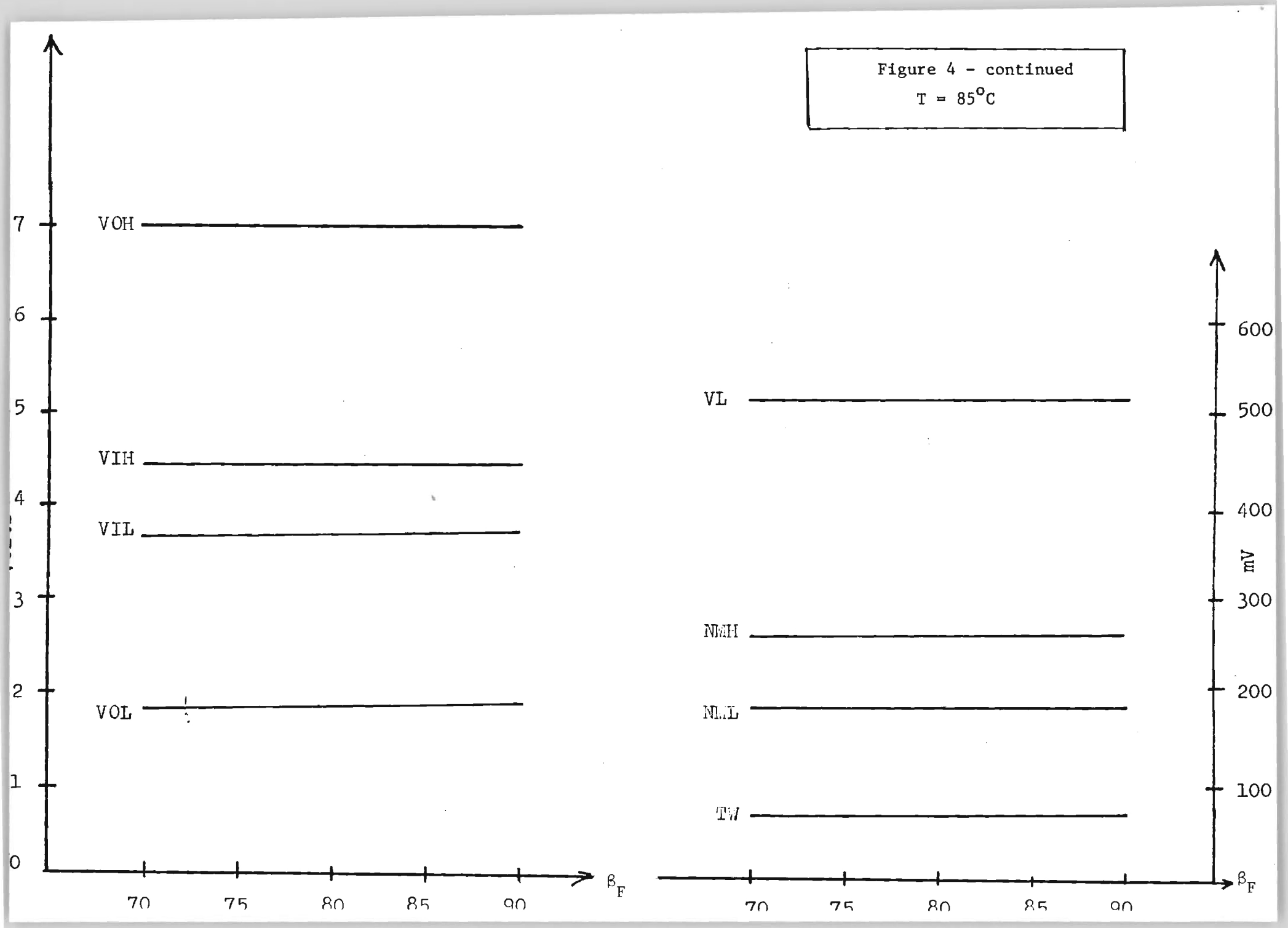


Figure 4 - continued
T = 85°C
7
6
5
4
3
2
1
0
VOH
VIH
VIL
VOL
70
75
80
85
90
β_F
VL
NMH
NML
TW
600
500
400
300
200
100
mV
β_F

function of the specific value β_F used to describe the current gain of Q1, Q2 and Q3.

Another series of graphs is presented in Fig. 5. These represent the variations in the digital voltage quantities as functions of the saturation current I_S. In the most basic model, I_S occurs in the forward-active current expression

$$I_C \simeq I_S \, e^{qV_{BE}/kT} \qquad (9)$$

which is sometimes termed the transfer equation. The SPICE simulation used to generate the graphs actually employs I_S in a more complete charge-control model which degenerates to the Ebers-Moll equivalent circuit. However, I_S has roughly the same meaning.

The behavior shown in these graphs indicates the complex dependence of the voltage quantities on the value of I_S. Since the saturation current is related to the Gummel number by approximate inverse proportionality

$$I_S \simeq \frac{1}{N_G} \quad , \qquad (10)$$

these variations illustrate the importance of the base doping profile. The relation between the Gummmel number N_G and the base doping profile $N_{aB}(x)$ is

$$N_G = \int_0^W N_{aB}(x) \, dx \qquad (11)$$

where W is the width of the quasi-neutral base region. Consequently,

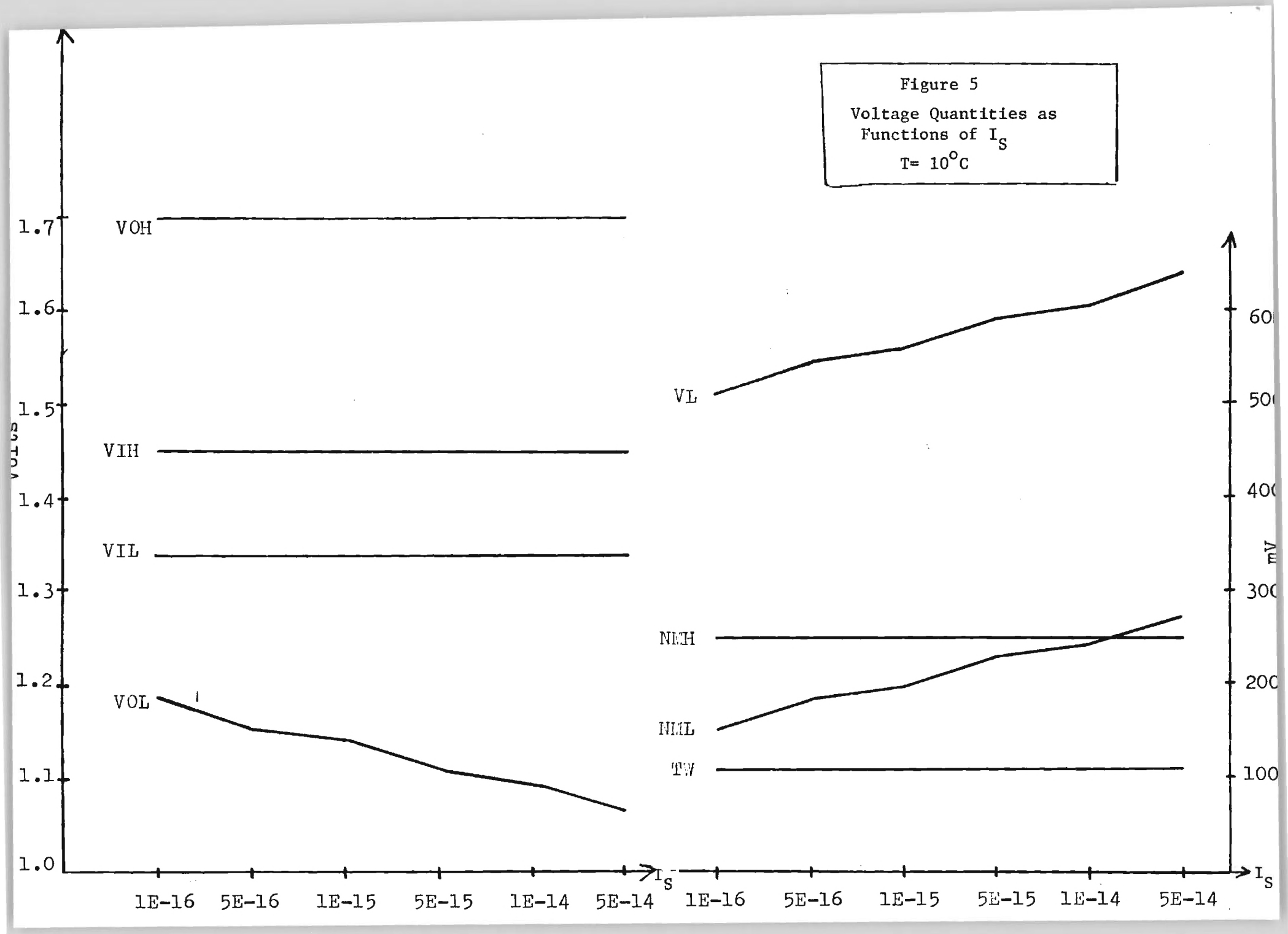


Figure 5
Voltage Quantities as Functions of I_S
T= 10°C
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
VOH
VIH
VIL
VOL
VL
NMH
NML
TW
60
50
40
30
20
10
mV
1E-16
5E-16
1E-15
5E-15
1E-14
5E-14
I_S

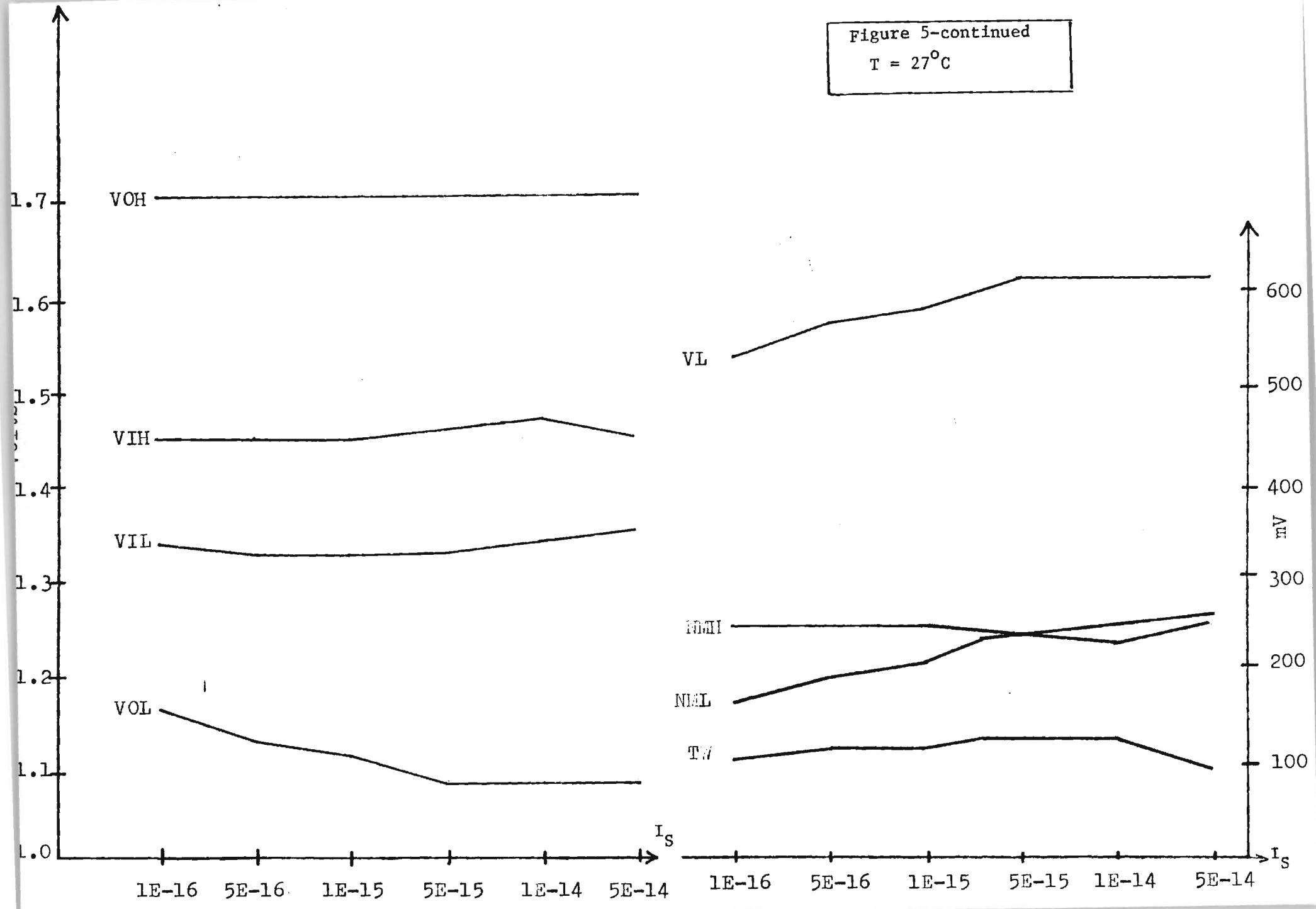


Figure 5-continued
T = 27°C
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
VOH
VIH
VIL
VOL
VL
NMH
NML
600
500
400
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mV
I_S
1E-16
5E-16
1E-15
5E-15
1E-14
5E-14

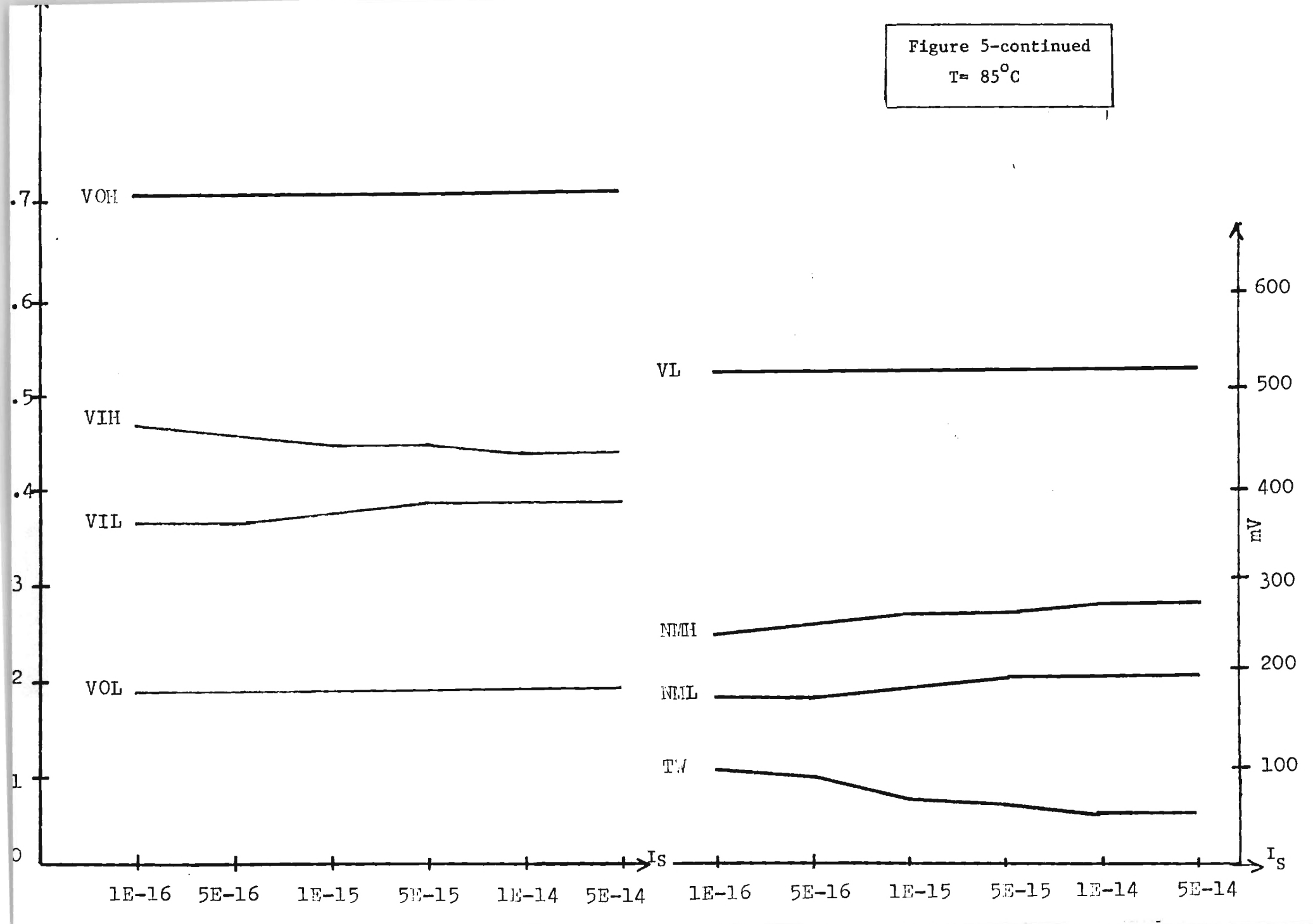
Figure 5-continued
T= 85°C
.7
.6
.5
.4
3
2
1
0
VOH
VIH
VIL
VOL
VL
NMH
NML
TW
600
500
400
300
200
100
mV
Is
Is
1E-16
5E-16
1E-15
5E-15
1E-14
5E-14
1E-16
5E-16
1E-15
5E-15
1E-14
5E-14

this analysis indicates the important interaction with the processing parameters as applied to the resulting circuit switching characteristics. Other intrinsic quantities such as the base resistance R_B have also been examined in the same context. The complete analysis of these variations will appear in the Final Report.

The effects of FanOut (FO) variations have also been examined using the SPICE simulation. These runs have been performed for various Fan In (FI) values with simplified RC-type modelling for the interconnect structures. Some of these results are presented in the next set of graphs, but will not be discussed in detail here. The analysis of the FO and FI variations is still under investigation, although a simplified linear-type dependence has been estimated for some voltage quantities.

This portion of the work is being extended to include all possible variations in the circuit which may lead to changes in the NM values. It has become apparent that the most significant variations arise when the base doping is changed (which leads to I_S modifications), and also when the shape of the current-voltage transistor curves are perturbed. The first observation appears to set a constraint on the design of the circuit which is based in the process variations, i.e., the 3σ spread. The latter is more dependent upon the modelling employed to simulate the circuit, but may have deeper roots. These problems will be studied during the final phases of the research.

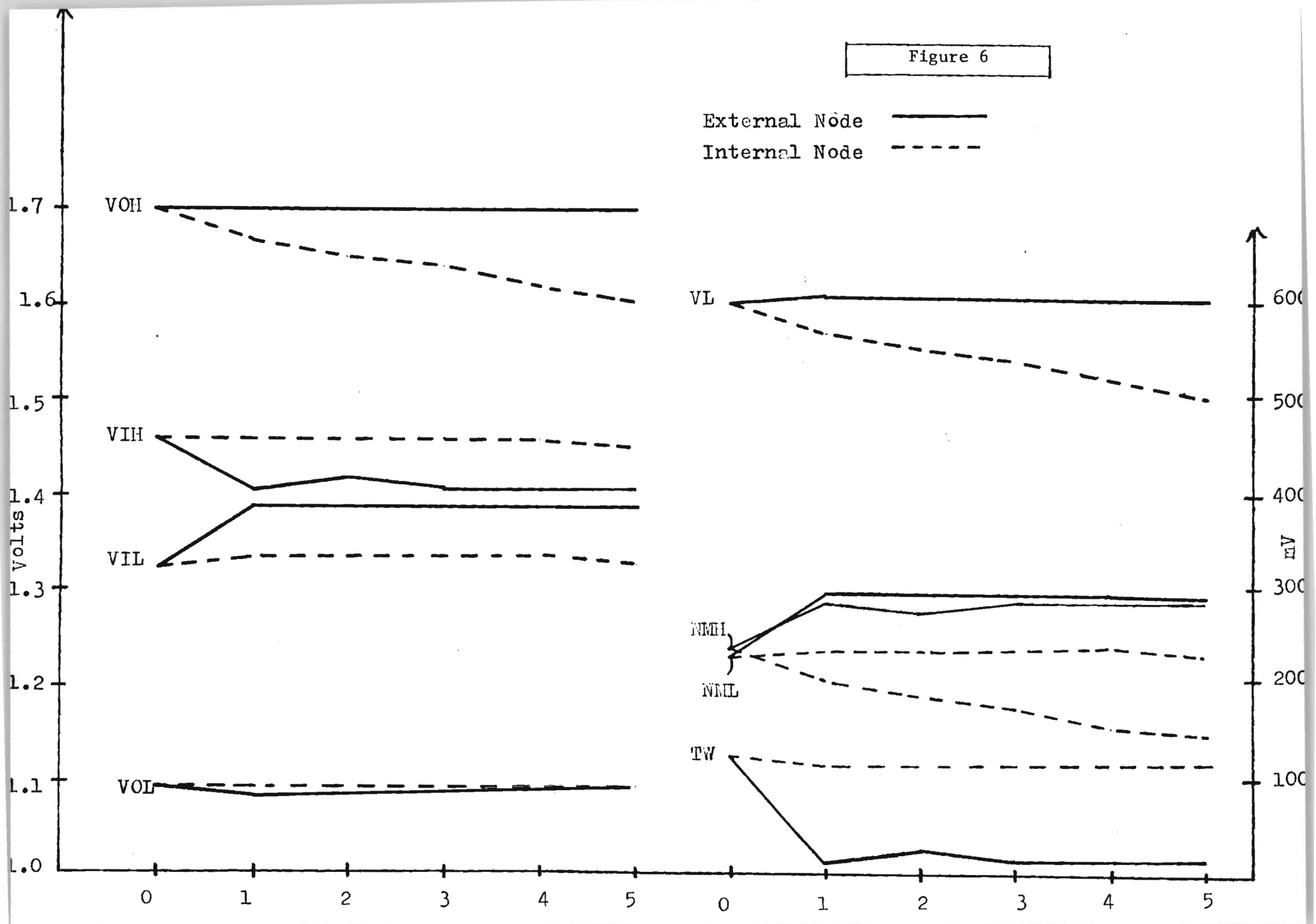
Figure 6
External Node
Internal Node
VOH
VIH
VIL
VOL
VL
NMH
NML
TW
Volts
mV
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
600
500
400
300
200
100
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1
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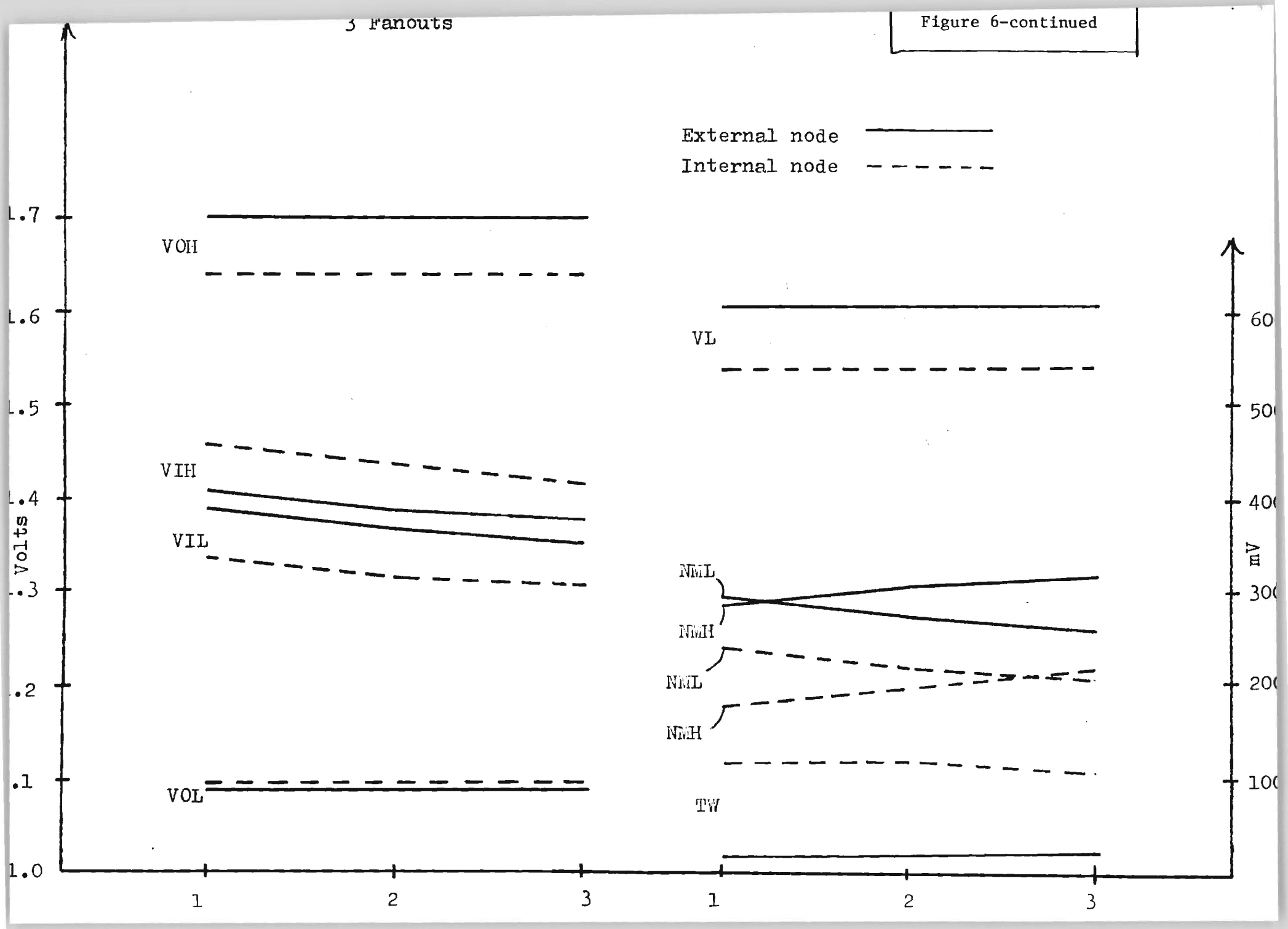

Figure 6-continued

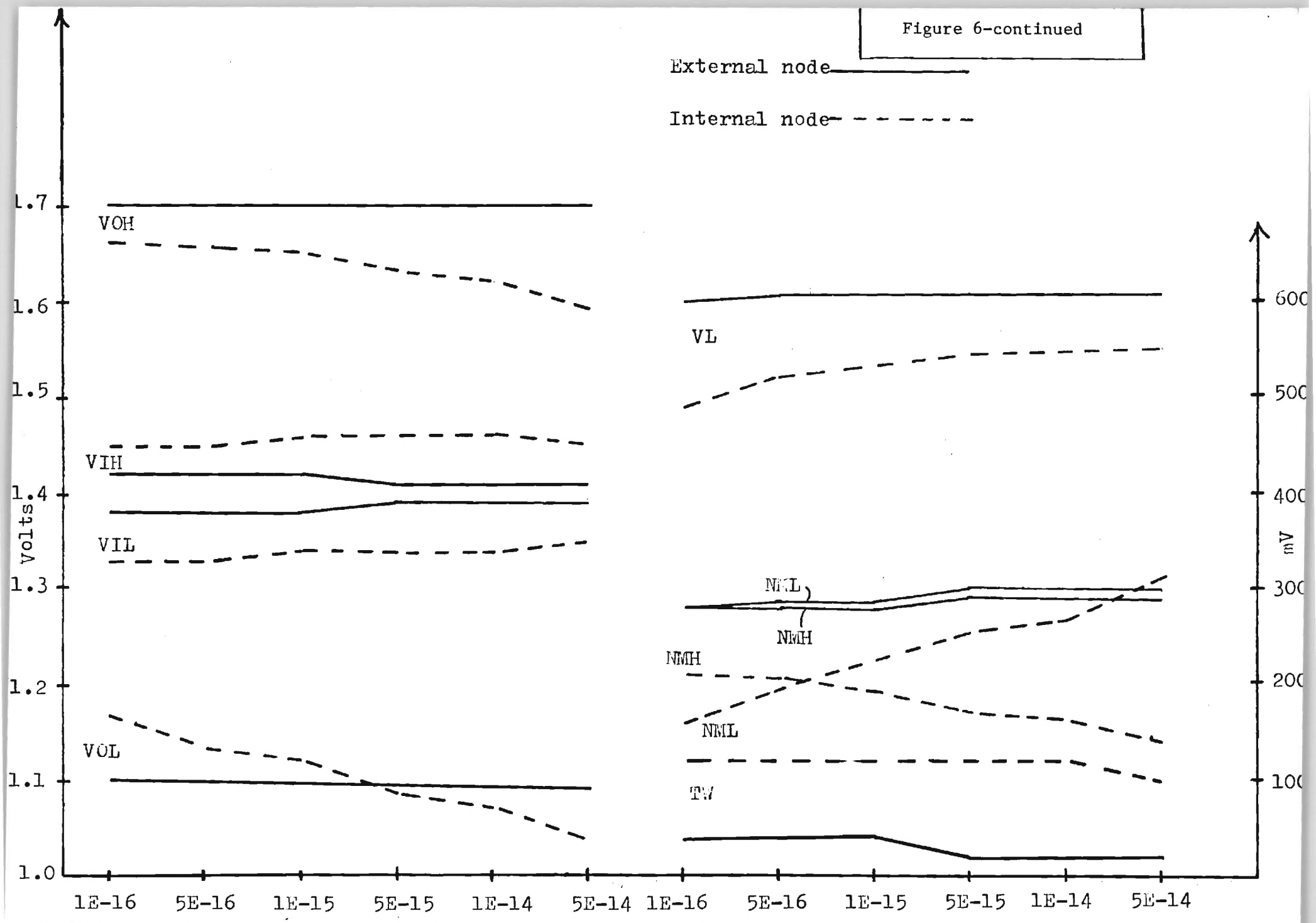
Figure 6-continued
External node
Internal node
VOH
VIH
VIL
VOL
VL
NML
NMH
NMH
NML
TW
Volts
mV
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
600
500
400
300
200
100
1E-16
5E-16
1E-15
5E-15
1E-14
5E-14
1E-16
5E-16
1E-15
5E-15
1E-14
5E-14

3. Charge-Control Modelling

Although the SPICE circuit simulations are useful for isolating the important depedences which lead to the formation of the circuit Noise Margin, it is not possible to make any conclusions until a more thorough analysis is performed. The important dependence of the Noise Margins I_S has led to modelling the basic switching problem using a charge-control approach for the transistor. This has the advantage that the Gummel number N_G can be directly related to the base charge. Consequently, the objective of this portion of the research has been to determine the sensitivity of the digital voltage quantities with regards to the base doping profile.

To outline the method being utilized, recall that the basic charge-control model for a bipolar transistor gives the collector current I_C a

$$I_C \simeq \frac{Q_F}{\tau_F} - \frac{dQ_{VC}}{dt} \qquad (12)$$

which is valid in forward-active bias. Q_F represents the "forward charge" in the base, and τ_F is the electron lifetime in this region. The voltage-dependent quantity Q_{VC} is the base-collector depletion charge, which changes during a switching event. Letting A be the emitter area and V_A the Early voltage, this can be written in the form

$$I_C \simeq \frac{qAN_G}{\tau_F} e^{qV_{BE}/kT} - \frac{AN_G}{N_{aB}(0)\ V_A} \frac{dQ_{VC}}{dW} \frac{dV_{BC}}{dt} \qquad (13)$$

where $N_{aB}(0)$ is the base doping density at the edge of the base-emitter depletion region.

The simplest analysis comes about by assuming a linearly graded base-collector junction with a grading constant of a. This is then combined with a simplified input voltage ramp of the form

$$V_{in}(t) = Bt \tag{14}$$

as a means of obtaining a first-order approximation for the input waveform. When these are included in the charge-control model for the basic ECL inverter, the resulting differential equation may be solved to yield

$$I_C \simeq qAN_G \left[\frac{2N_a(W)\ V_A\ (kT/q)\ e^{qV_{BE}/kT}}{\tau_F[aBqAN_G W_{BC} R_C + 2N_a(W)\ V_A\ (kT/q)]} - \frac{aBW_{BC}}{2N_a(W)V_A} \right] \tag{15}$$

where W_{BC} represents the voltage-dependent base-collector depeletion width. Although somewhat complicated looking, this equation has been compared with the simplified SPICE model, where the two may be correlated. The circuit properties are then extracted by relating the level of collector current to the output voltage by a simple application of Ohm's Law; it is found necessary to invoke some circuit approximations to attain a simple closed-form expression.

This analysis is still in progress. As can be seen from the basic charge-control equation modelling, the analytical analysis of the problem can get somewhat involved. However, the basic dependences are starting to manifest themselves in terms of the saturation currents and termperature terms. The Final Report will contain the details of the analysis and the conclusions concerning the NM and supply levels which may be used.

4. Noise Sources

The newest problem to be examined in the research centers around the problem of noise sources within the transistors themselves. The basic device model is illustrated in Fig. 7, and is based upon the small-signal hybrid-pi for simplicity. Once this is analyzed in detail, it is possible to extract the large-signal digital properties which are modified by the presence of intrinsic and induced noise sources.

The initial stages of this phase of work have centered around finding the explicit dependence of the collector current on the noise sources denoted by $|\overline{V_B}^2|$, $|i_B|^2$ and $|i_c|^2$ in the equivalent circuit. Although these are, in the strictest sense, small-signal sources, they can affect the switching of the network if the noise immunity of the configuration is low.

Work to this point has resulted in an expression for the DC collector current I_C as a function of the noise source amplitudes. This is quite complicated, and will not be reproduced here. It will, however, appear in the Final Report. The transient response problem is being investigated by means of a nodal response simulation which employs both the small-signal and large-signal characteristics of the transistor. In addition, the problem of noise generation by passive elements in the circuits is being included in the modelling.

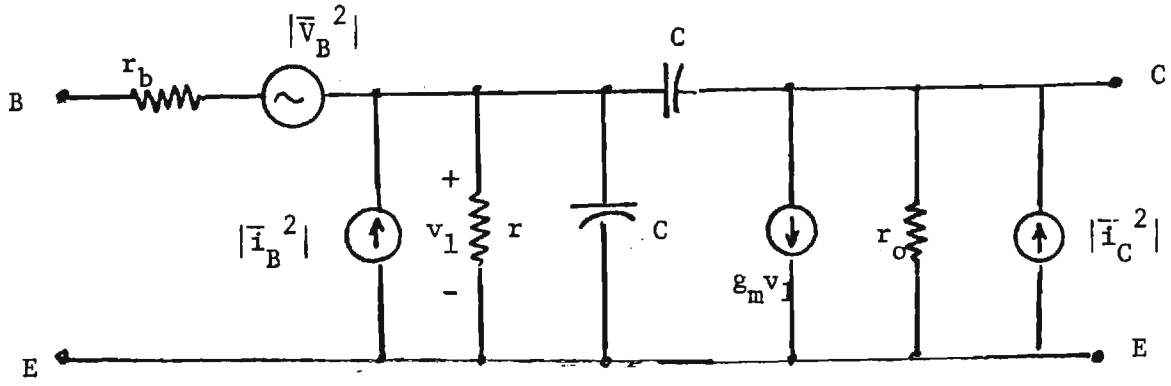

Figure 7

Basic Noise Model for Transistor

5. Program for Remaining Work

The summary here has briefly presented some of the more important aspects of the research performed to this point. Some of the topics under investigation have not been dealt with in detail. This includes items such as the noise margin for off-chip driver circuits. Although each of the sub-studies can be analyzed in more detail, it is felt that the work already completed forms a substantial basis for understanding the basic problems of NM formation and minimum power supply levels.

The remaining efforts will thus be directed to correlating the results in an approximately consistent manner for the purpose of obtaining design recommendations. The preliminary studies in this area appear to be headed in the right direction, with major functional dependences being extracted in the form of proportionalities. Although a more exacting analysis is desired, the proportionalities allow one to base future designs on existing circuit measurements.

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GEORGIA INSTITUTE OF TECHNOLOGY
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NE: (404) 894-2961

December 20, 1984

Mr. D. B. Mooney
D/29A, Zip 47A
IBM General Technology Division
East Fishkill Facility
Route 52
Hopewell Junction, NY 12533

SUBJECT: Quarterly Report, IBM Purchase Order No. 7S-785515, Project Director - J. P. Uyemura, Project Entitled, "Physical Limitations on Bipolar Digital Integrated Circuits," Period of Performance - 7/1/84 - 9/15/84

Dear Mr. Mooney:

Enclosed is the final quarterly report for the subject IBM purchase order. The period covered by this report is July 1, 1984 - September 15, 1984. I apologize for being late with the report, but Dr. Uyemura has been quite ill during the past few months.

If you have any questions or comments concerning this report, please contact Dr. John P. Uyemura at 404/894-2975.

Sincerely,

Cindy Meyer
Admin. Asst.

CM

cc: J. P. Uyemura
OCA (2)

PHYSICAL LIMITATIONS on BIPOLAR DIGITAL INTEGRATED CIRCUITS

FINAL REPORT

John P. Uyemura
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, GA 30332

ABSTRACT

The problem of noise margin formation in ECL integrated circuits is studied. The important device parameters are isolated and analyzed, and the question of power supply levels is addressed. It is found that it is not possible to develop any simplistic circuit or chip design procedures. However, step-by-step guidelines do exist, and can be applied to the design problem.

TABLE OF CONTENTS

1. Introduction

The research described in this report deals with the problem of noise margin formation in digital bipolar integrated circuits. The primary area of research centered around computing critical switching voltages in a simplified ECL configuration and studying the device and circuit parameters which were most influential in setting the final numerical values.

Much of the work discussed here employed the well-known circuit simulation program SPICE (Simulation Program with Integrated Circuit Emphasis) to deduce the initial characteristics. It is assumed that the reader is familiar with this program, in addition to having a reasonable background in device physics and circuit design.

Chapter 2 is included to establish the basic voltage conventions employed throughout the report. The device modelling in Chapter 3 also falls in this category.

The circuit analysis of the basic ECL current switch is the subject of Chapter 4. This is extended to the OR/NOR configuration in Chapter 5.

The major portion of the research starts with Chapter 6 which is concerned with computing the critical switching voltages of the ECL OR/NOR circuit as functions of various SPICE parameters. This set of data allows for extracting the most important device parameters which influence the digital voltage levels. The results are subjected to an analytical treatment in Chapter 7, which also includes a discussion of the minimum power supply voltage factors. These two chapters constitute the most important results of the research.

Chapter 8 deals with the development of a charge-control model for the ECL circuit. This is done in a purely analytic approach.

Chapter 9 repeats the material covered in Chapters 6 and 7 for the variations due to FanOut (FO) changes. The FO is found to be very important for determining noise margins and digital logic levels, and a set of theoretical equations are developed to predict these values.

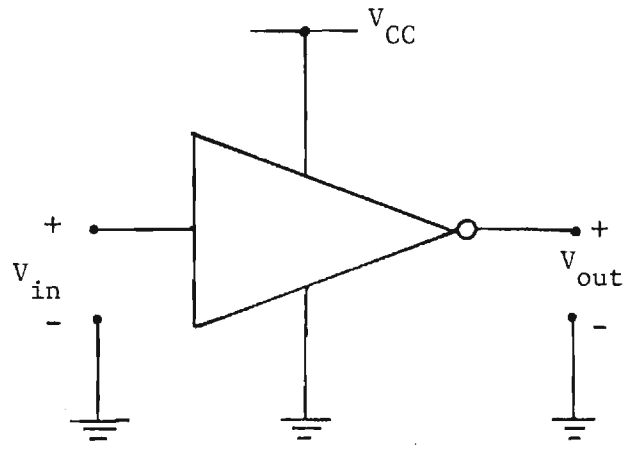
Chapter 10 summarizes the problem of interconnect coupling using both circuit and transmission line analysis.

2. Voltage Levels in Digital Circuits

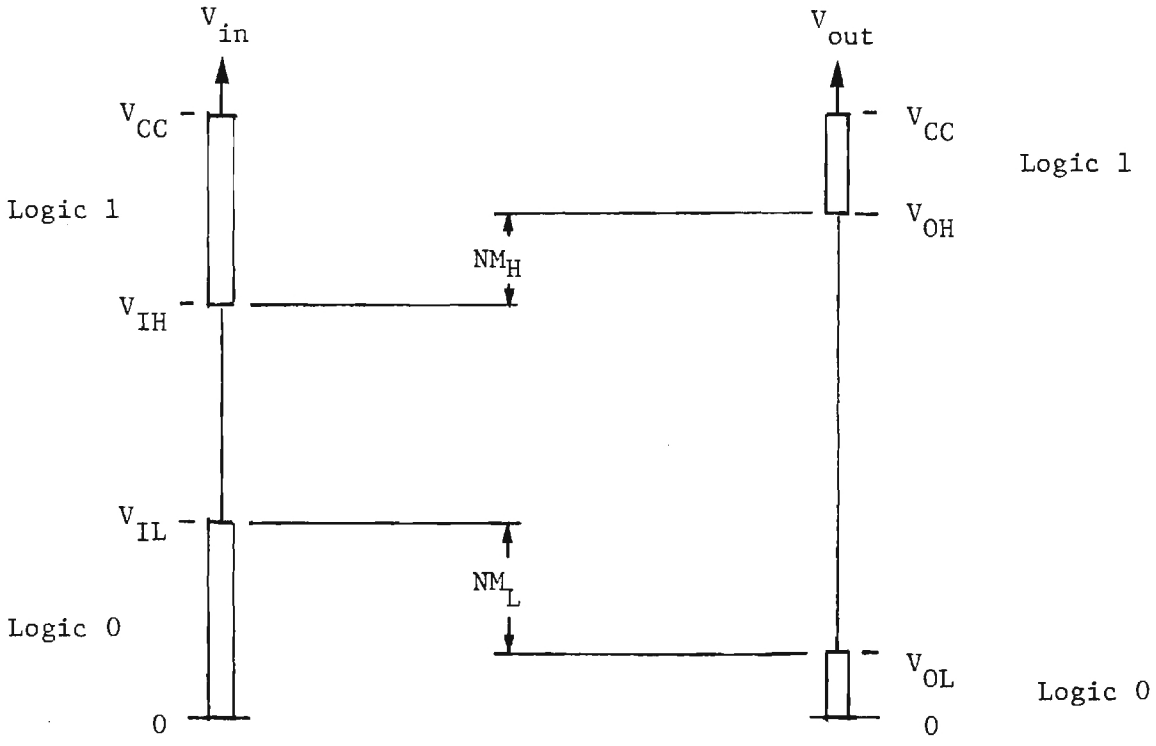
The discussion here will use standard voltage definitions to describe the switching properties of digital bipolar integrated circuits. The basic problem is illustrated in Fig. 1 which shows an inverter stage with a power supply level of V_{CC}. Owing to the fact that voltages are not quantized in nature, the internal circuit nodes of the inverter may be at any value between 0 and V_{CC}, depending upon the value of the input voltage V_{in}. To describe Boolean logic 0 and 1 levels, it is necessary to assign voltage ranges to V_{in} and V_{out} which correspond to the desired binary coding. Although these are obtained from an inverter, they are assumed to be generally valid for any digital switching network. The treatment will employ a positive logic convention in which the larger (more positive) voltage represents a logic 1 state.

The voltage ranges used to describe digital circuits are based on the performance of a ring oscillator obtained by creating a closed loop of cascaded inverters with an odd number of stages. The input voltage V_{in} is thus related to the output voltage of the previous stage. The input voltage has associated with it two important levels. These are V_{IH}, the "input high" voltage, and V_{IL}, the "input low" voltage. As shown in Fig. 1(b), these are used to define the input logic levels by means of

$$\begin{aligned} &\text{Input Logic 1:} \quad V_{IH} \text{ to } V_{CC} \\ &\text{Input Logic 0:} \quad 0 \text{ to } V_{IL} \ . \end{aligned} \tag{2-1}$$



Gate Symbol
(a)



Voltage Definitions
(b)

Figure 1
Basic Digital Logic Voltage Definitions

It is seen that V_{IH} represents the lowest input voltage which will be interpreted as a logic 1 state, while V_{IL} is the largest value of V_{in} which represents a logic 0. The input "transition width" TW is then given by

$$TW = V_{IH} - V_{IL} \tag{2-2}$$

and gives the separation between the input logic states.

The output voltage V_{out} is defined using similar voltage levels. These are denoted by V_{OH}, the "output high" voltage, and V_{OL}, the "output low" voltage. The output logic levels are defined by

$$\begin{aligned} &\text{Output Logic 1:} \quad V_{OH} \text{ to } V_{CC} \\ &\text{Output Logic 0:} \quad 0 \text{ to } V_{OL} \, . \end{aligned} \tag{2-3}$$

V_{OH} is seen to be the smallest value of V_{out} which represents a logic 1 state, while V_{OL} is the largest logic 0 output value. The output "logic swing" V_{ℓ} is given by

$$V_{\ell} = V_{OH} - V_{OL} \tag{2-4}$$

and is one of the most important voltage differences in the circuit. In particular, an ideal inverter would have $V_{\ell} = V_{CC}$ which would indicate perfect wave shaping by the gate.

The circuit "noise margins" are defined by the relative voltage

differences between input and output logic levels. The high (logic 1) noise margin NM_H is given as

$$NM_H = V_{OH} - V_{IH} \tag{2-5}$$

while the low (logic 0) noise margin NM_L is defined by

$$NM_L = V_{IL} - V_{OL} \quad . \tag{2-6}$$

The noise margins are shown in Fig. 1(b). A functional circuit requires that both NM_H and NM_L be positive quantities, i.e., $V_{OH} > V_{IH}$ and $V_{IL} > V_{OL}$. This requirement is easily understood by examining the criteria for oscillation in the cascaded inverter circuit. It is noted in passing that zero noise margins would theoretically be acceptable; hpwever, a realistic circuit would not be functional because of normal processing variations.

The actual switching characteristics of an inverter are described by the "Voltage Transfer Characteristic" (VTC) shown in Fig. 2. This is simply a plot of V_{out} as a function of V_{in}, and is analogous to the "S-Curve" plot for a buffer (amplifier) stage. It is seen that the critical output voltages V_{OH} and V_{OL} are easily obtained from inspection of the V_{out} limits. The critical input voltages V_{IL} and V_{IH} are a bit more complicated. They are usually defined by the points where

$$\frac{dV_{out}}{dV_{in}} = -1 \quad , \tag{2-7}$$

i.e., where the slope of the VTC is -45^{o}. The "unity gain line"

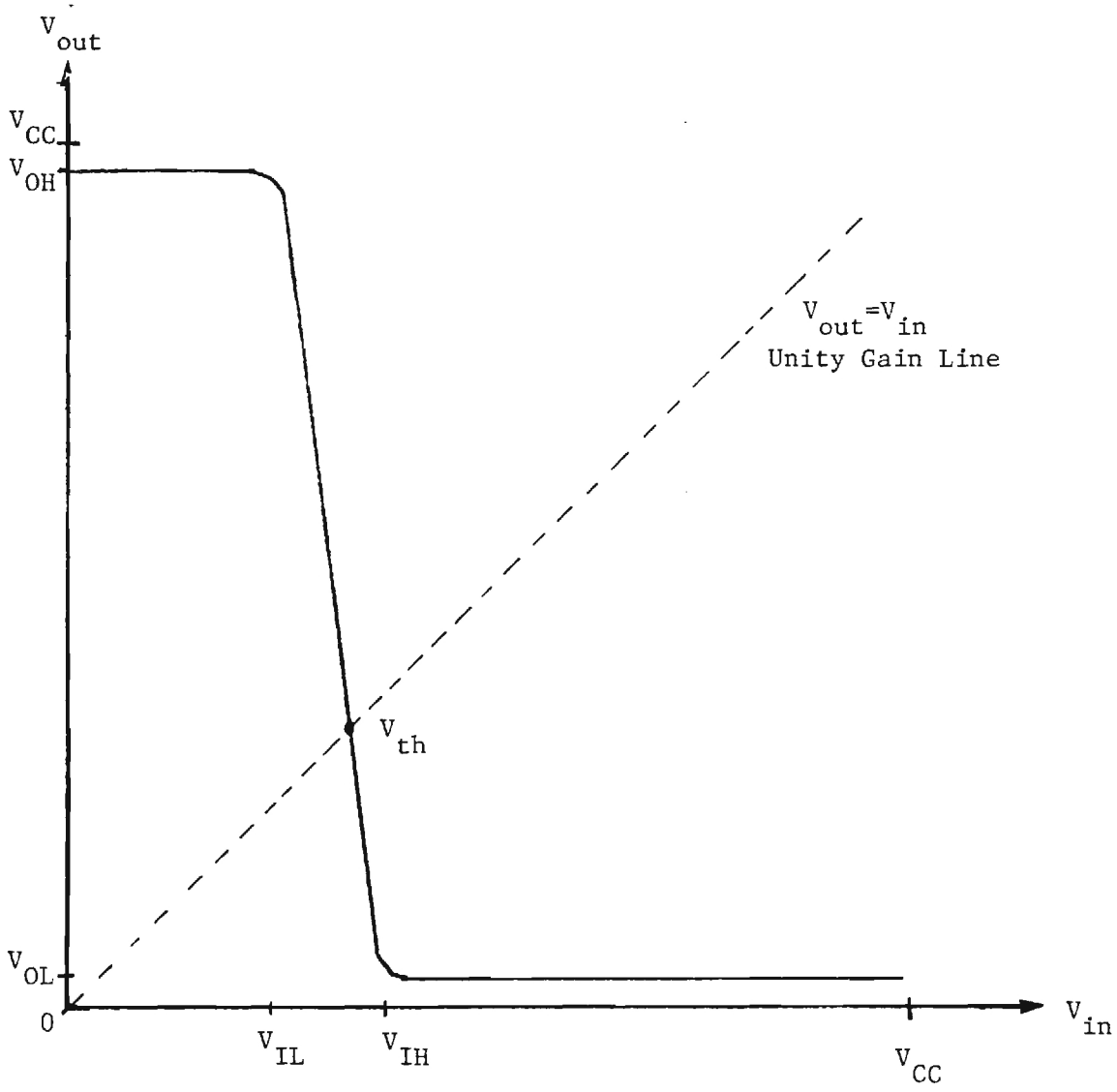


Figure 2

Basic Voltage Transfer Characteristic
Inverter Curve

where $V_{out} = V_{in}$ is shown as a dotted line in the VTC drawing. The "inverter threshold" voltage V_{th} is then taken as the point on the VTC where

$$V_{out} = V_{in} = V_{th} \tag{2-8}$$

is satisfied. V_{th} is thus a measure of the voltage gain provided by the circuit under consideration.

The inverter threshold is used to define the "noise sensitivity" by means of

$$\begin{aligned} NS_L &= V_{th} - V_{OL} \\ NS_H &= V_{OH} - V_{th} \quad . \end{aligned} \tag{2-9}$$

For an ideal inverter, $NS_H = NS_L = (V_{CC}/2)$. These quantities are interpreted as the amount of voltage necessary at the input to induce a transition in the gate. The "noise immunities" are then defined by

$$\begin{aligned} NI_L &= \frac{NS_L}{V_\ell} \\ NI_H &= \frac{NS_H}{V_\ell} \end{aligned} \tag{2-10}$$

and represent convenient measures of the circuit's ability to reject noise (or spurious interference) signals.

3. Device Modelling

The analysis here employs two basic levels of bipolar transistor modelling. The simplest of these is the large-signal Ebers-Moll equivalent circuit, which is useful in analytic switching descriptions. The more complex charge-control equations may be used to a limited degree in analytic circuit analyses, but are complicated enough to usually restrict their usage to computer simulations. Both levels of modelling are summarized in this section.

3.1 Ebers-Moll Equivalent Circuit

The large-signal Ebers-Moll equivalent circuit is illustrated in Fig. 3 for an npn transistor. The equations describing the terminal currents are

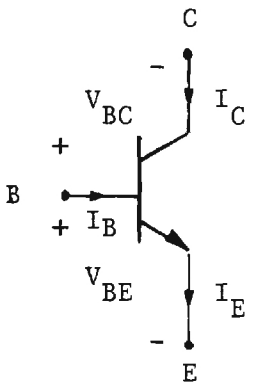
$$I_E = I_{ES}(e^{V_{BE}/V_T} - 1) - \alpha_R I_{CS}(e^{V_{BC}/V_T} - 1)$$

$$I_C = \alpha_F I_{ES}(e^{V_{BE}/V_T} - 1) - I_{CS}(e^{V_{BC}/V_T} - 1) \qquad (3.1\text{-}1)$$

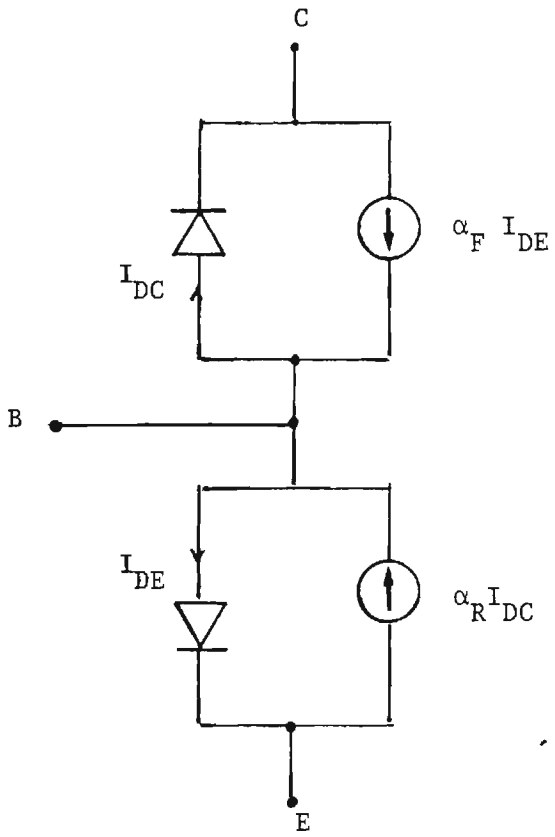
and $I_B = I_E - I_C$. In these equations, $V_T = (kT/q)$ represents the thermal voltage, while α_F and α_R respectively denote the forward and reverse alphas (common-base current gain). I_{ES} is the emitter saturation current and I_{CS} is the collector saturation current. Typical orders of magnitudes assumed in the analysis are

$$\alpha_F \simeq 0.99 \quad , \qquad \alpha_R \simeq 0.67 \; . \qquad (3.1\text{-}2)$$

The saturation currents are on the order of a few femptoamperes [fA]. It is assumed that reciprocity in the form



Current and Voltage
Definitions
(a)



Basic Model
(b)

Figure 3

Ebers-Moll Equivalent

$$\alpha_F I_{ES} = \alpha_R I_{CS} \tag{3.1-3}$$

is valid in the analysis.

The operational modes of the bipolar transistor are described by the terminal voltages V_{BE} and V_{BC} in the Ebers-Moll equivalent circuit. The forward-active mode is of particular interest. This occurs when the base-emitter junction is forward-biased ($V_{BE} > 0$) and the base-collector junction is reverse-biased ($V_{BC} < 0$). Assuming that the junction bias voltages are much larger in magnitude than the thermal voltage reduces the equations to the approximate forms

$$I_E \simeq I_{ES} e^{V_{BE}/V_T} + \alpha_R I_{CS}$$

$$I_C \simeq \alpha_F I_{ES} e^{V_{BE}/V_T} + I_{CS} \quad . \tag{3.1-4}$$

An alternate form for the collector current in this operational mode is

$$I_C = \alpha_F I_E + I_{CO} \tag{3.1-5}$$

where

$$I_{CO} = I_{CS}(1 - \alpha_R \alpha_F) \quad . \tag{3.1-6}$$

In terms of the common-emitter forward current gain β_F, this is

$$I_C = \beta_F I_B + (\beta_F + 1)\, I_{CO} \qquad (3.1\text{-}7)$$

with the usual definition

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \quad . \qquad (3.1\text{-}8)$$

The Ebers-Moll equations are primarily based on the simplistic diode model shown in Fig. 3. In order to more closely describe the device physics of the transistor, it is common to define the basic saturation current I_S in the form

$$I_S = \alpha_F I_{ES} = \alpha_R I_{CS} \quad . \qquad (3.1\text{-}9)$$

This reduces the terminal currents to

$$I_E = \frac{I_S}{\alpha_F}(e^{V_{BE}/V_T} - 1) - I_S\,(e^{V_{BC}/V_T} - 1)$$

$$I_C = I_S(e^{V_{BE}/V_T} - 1) - \frac{I_S}{\alpha_R}\,(e^{V_{BC}/V_T} - 1) \qquad (3.1\text{-}10)$$

for arbitrary voltages V_{BE} and V_{BC} . In forward-active bias, the currents are approximated by means of

$$I_E \simeq \frac{I_S}{\alpha_F}\, e^{V_{BE}/V_T}$$

$$I_C \simeq I_S\, e^{V_{BE}/V_T} \qquad (3.1\text{-}11)$$

which allows for a direct connection with the electron transport analysis.

A typical oxide-isolated bipolar transistor structure is shown in Fig. 4. The mechanism of electron transport under forward-active bias is easily seen from the drawing. Electrons originate from the emitter n^+ well and are injected across the foward-biased base-emitter junction into the quasi-neutral base region. Since the p-type base region will have a doping gradient associated with it (from either an impurity diffusion or an ion implantation), the electrons will traverse the base region by both drift and diffusion. Electrons which make it across the base without undergoing a recombination event with the majority carrier holes are then swept up by the large depletion electric field in the reverse-biased base-collector junction. This then gives the collector current.

In the lowest-order of approximation, the electron transport in the base can be analyzed using the generic doping profile shown in Fig. 5. The important dependence is $N_a(x)$, as this gives both the built-in electric field for the drift component, and it also sets the point-by-point values of the diffusion coefficient. The results of the device analysis gives a saturation current in the form

$$I_S = \frac{qA_E \tilde{D}_n n_i^2}{N_G} \qquad (3.1\text{-}12)$$

where $q = 1.6 \times 10^{-19}$ [C] is the basic charge unit, A_E is the emitter area perpendicular to the diregion of current flow, $\tilde{D}_n$ is the average electron diffusion coefficient in the base, and n_i is the temperature-

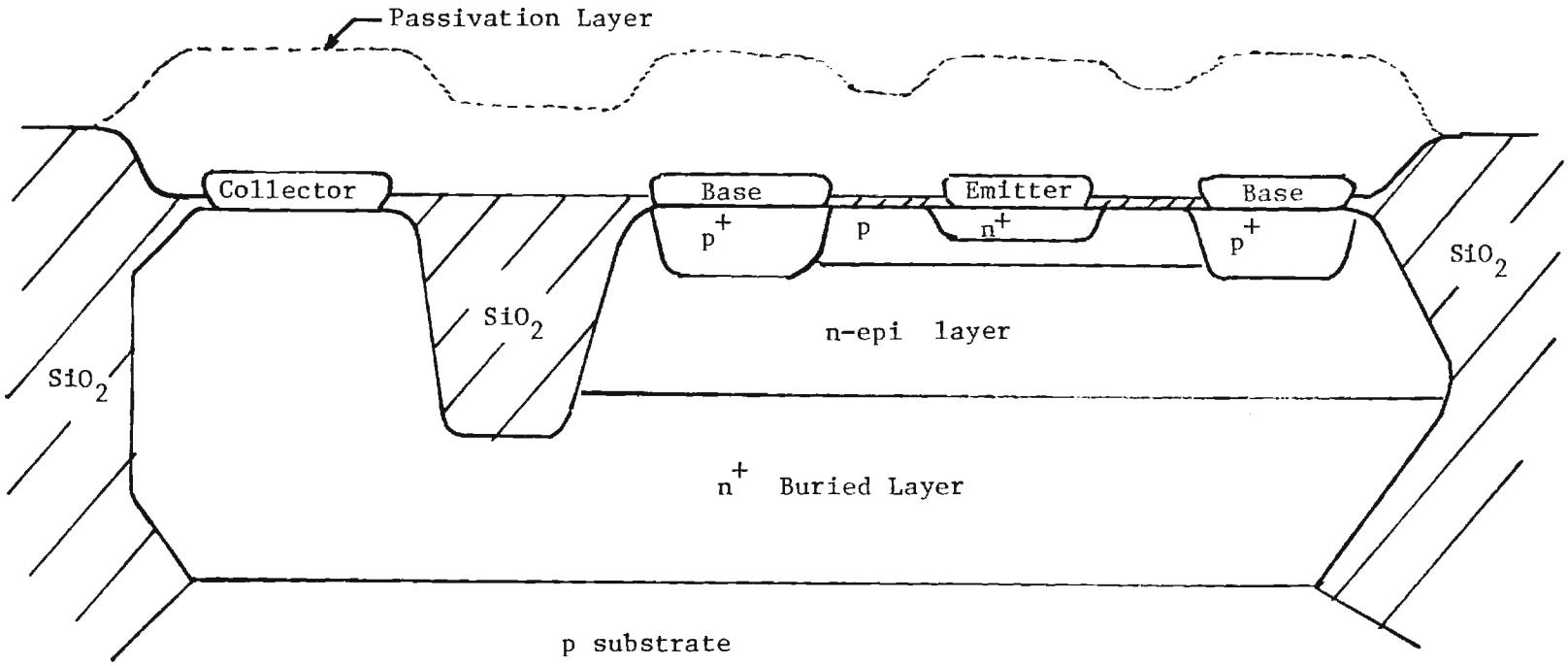


Figure 4

Basic Oxide-Isolated Bipolar
Transistor Cross-Section

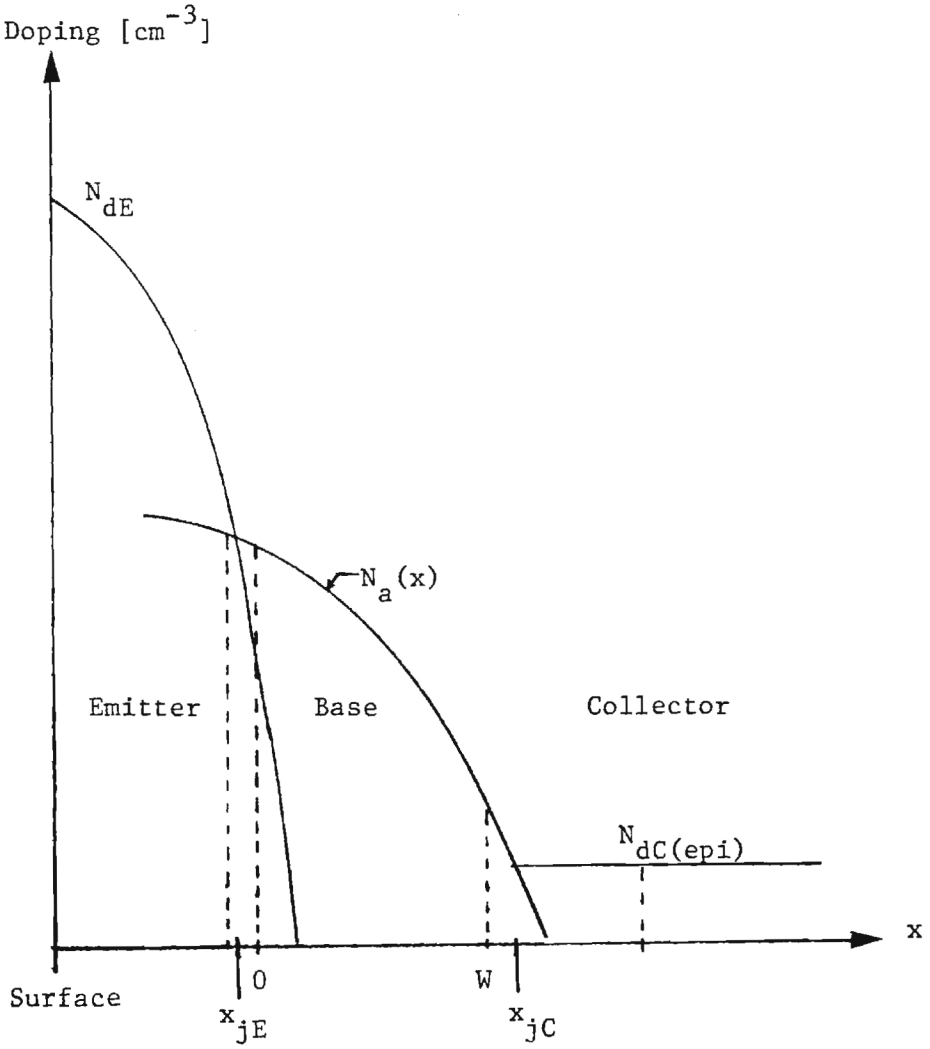


Figure 5

Basic Doping Profile for
npn Transistor

dependent intrinsic concentration (assumed to be 1.45 x 10^{10} [cm^{-3}] for silicon at 27° C). N_G is used here to denote the Gummel number such that

$$N_G = \int_0^W N_a(x)\, dx \qquad [cm^{-2}] \tag{3.1-13}$$

where W is the quasi-neutral base width under the specified bias levels. As will be seen later in the discussion, the Gummel number is an extremely important parameter when discussing the switching properties of digital circuits.

3.2 Charge-Control Models

The charge-control approach to describing bipolar transistors accounts for both charge motion (current) and charge storage in the device. The basic npn charge-control model is illustrated in Fig. 6 where it is seen that the model employs non-linear capacitors in addition to the diodes and current sources found in the Ebers-Moll model. The model is useful for both DC and transient analysis.

The equations of the charge-control equivalent circuit are given in the form

$$i_C = \frac{Q_F}{\tau_F} - Q_R\left(\frac{1}{\tau_R} + \frac{1}{\tau_{BR}}\right) - \frac{dQ_R}{dt} - \frac{dQ_{VC}}{dt}$$

$$i_B = \frac{Q_F}{\tau_{BF}} + \frac{dQ_F}{dt} + \frac{dQ_R}{\tau_{BR}} + \frac{dQ_{VC}}{dt} + \frac{dQ_{VE}}{dt} \tag{3.2-1}$$

and $i_E = i_B + i_C$. In these equations, Q represents various charges

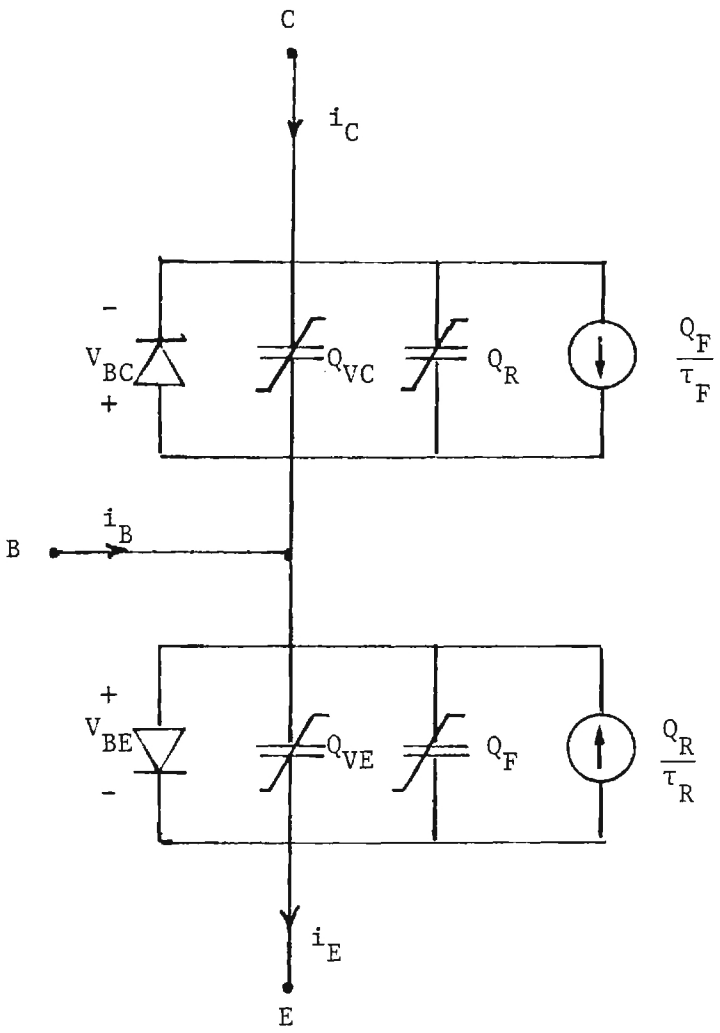


Figure 6

Charge-Control Model for an
npn Transistor

It is interesting to note that if the ratio of ΔI_S to $\Delta \eta_F$ is

$$\frac{\Delta I_S}{\Delta \eta_F} \simeq \frac{I_S V_{BE}}{\eta_F V_T} \tag{7-5}$$

then this equation predicts $\Delta I_C \simeq 0$ because of compensation. This, of course, is highly unlikely in the real world.

To understand the meaning and content of this set of equations, recall that a low-order approximation for the saturation current is

$$I_S \simeq \frac{q A_E \tilde{D}_n n_i^2}{N_G} \tag{7-6}$$

as verified from eqn. (3.1-12). The Gummel number N_G was given as

$$N_G = \int_0^W N_a(x)\, dx \tag{7-7}$$

where $N_a(x)$ is the net acceptor doping in the base p-type layer, and W is the width of the quasi-neutral base region. N_G is the primary processing and operational variable in the saturation current. Thus, variations in I_S based upon Gummel number changes gives

$$\Delta I_S \simeq - \frac{q A_E \tilde{D}_n n_i^2}{N_G^2} (\Delta N_G)$$

$$\simeq - I_S \frac{\Delta N_G}{N_G} \quad . \tag{7-8}$$

which are included in the analysis. The basic charge quantities are the foward and reverse charges Q_F and Q_R where

$$Q_F = Q_{FO}(e^{V_{BE}/V_T} - 1)$$
$$Q_R = Q_{RO}(e^{V_{BC}/V_T} - 1) \qquad (3.2\text{-}2)$$

describe current through the diodes. In these equations,

$$Q_{FO} = \frac{1}{2} q A_E W n_{po}$$
$$Q_{RO} = \frac{1}{2} q A_C W n_{po} \qquad (3.2\text{-}3)$$

where A_C is the collector area and n_{po} the equilibrium base minority carrier density. τ_F is the forward base transit time and represents the average time that an electron is in the quasi-neutral base region under forward-active oepration. τ_R is the analogous time interval for reverse-active operation. It is easily shown that the relationship to the Ebers-Moll model is provided by

$$Q_{FO} = \alpha_F I_{ES} \tau_F$$
$$Q_{RO} = \alpha_R I_{CS} \tau_R \qquad (3.2\text{-}4)$$

in the lowest order of approximation. The characteristic time intervals τ_{BF} and τ_{BR} represent effective base times in forward and reverse active bias to account for base recombination currents and hole injection from the base into an n-type region.

The only remaining charges which must be discussed are Q_{VC} and

Q_{VE}. These are nonlinear charges associated with the collector and emitter depletion regions. Complete modelling of these quantities requires knowledge of the junction doping profiles. Owing to the fact that these are usually quite complicated, hand calculations with the charge-control models are performed with step or linearly graded junction approximations.

The model employed by the SPICE circuit program is based on the charge control model. The important charges used to compute the circuit performance are usually denoted by Q_{BE} and Q_{BC} . Explicitly, these are given by

$$Q_{BE} = \tau_F I_S (e^{V_{BE}/V_T} - 1) + C_{jeo} \int_0^{V_{BE}} [1 - \frac{V}{\phi_e}]^{-m_e} \, dV$$

$$Q_{BC} = \tau_R I_S (e^{V_{BC}/V_T} - 1) + C_{jco} \int_0^{V_{BC}} [1 - \frac{V}{\phi_c}]^{-m_c} \, dV \qquad (3.2\text{-}5)$$

where ϕ_e and ϕ_c are respectively the base-emitter and base-collector built-in voltages. The quantities m_e and m_c are used to define the characteristics of the base-emitter and base-collector junction; with this form, m = (1/2) corresponds to a step profile, while m=(1/3) is a simple linearly graded pn doping profile. C_{jeo} and C_{jco} are the zero-bias depletion capacitance values.

4. ECL Current Switch Analysis

This section will present the analysis required to understand the switching properties of the basic ECL inverter/amplifier current switch shown in Fig. 7. The circuit consists of a balanced emitter-coupled pair where it is assumed that Q1 and Q2 are identical.

The VTC of the circuit is obtained by straightforward techniques. First, note that the output voltages are given by

$$V_{out,1} = V_{CC} - I_{C1}R_C$$

$$V_{out,2} = V_{CC} - I_{C2}R_C \quad . \tag{4-1}$$

Applying KCL at the emitter node gives

$$I_{E1} + I_{E2} = I_{EE} = \alpha_F(I_{C1} + I_{C2}) \tag{4-2}$$

which is a constant. The current flow on each side of the circuit can be obtained by noting that

$$V_{BE,1} = V_{in} - V_E$$

$$V_{BE,2} = V_R - V_E \tag{4-3}$$

where V_E is the emitter node voltage, and V_R is the reference voltage applied to the base of Q2. Using the forward-active Ebers-Moll equations from (3.1-4) then gives

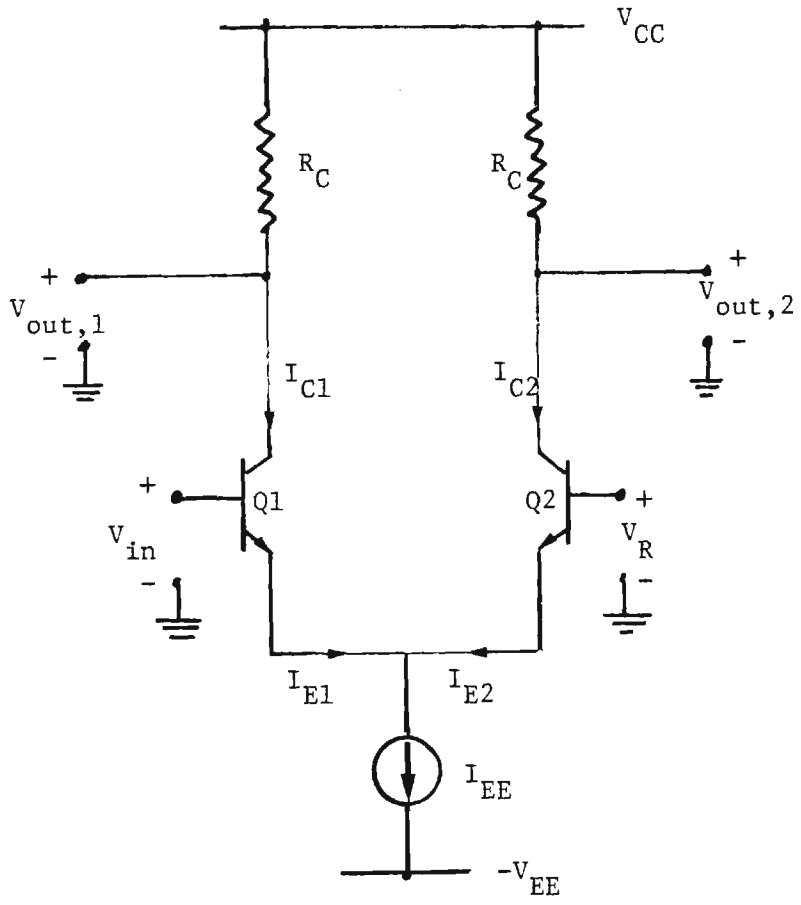


Figure 7

ECL Current Switch

$$I_{E1} = I_{ES}\, e^{(V_{in}-V_E)/V_T}$$

$$I_{E2} = I_{ES}\, e^{(V_R-V_E)/V_T} \qquad (4\text{-}4)$$

so that

$$\frac{I_{E1}}{I_{E2}} = e^{(V_{in}-V_R)/V_T} \qquad (4\text{-}5)$$

gives the ratio of emitter currents in terms of the voltage difference $(V_{in} - V_R)$. Combining this results with eqn. (4-2) then gives

$$I_{E1} = \frac{I_{EE}}{1 + e^{-(V_{in}-V_R)/V_T}}$$

$$I_{E2} = \frac{I_{EE}}{1 + e^{(V_{in}-V_R)/V_T}} \qquad (4\text{-}6)$$

Thus, the output voltages are obtained as

$$V_{out,1} = V_{CC} - \frac{\alpha_F I_{EE} R_C}{1 + e^{-(V_{in}-V_R)/V_T}}$$

$$V_{out,2} = V_{CC} - \frac{\alpha_F I_{EE} R_C}{1 + e^{(V_{in}-V_R)/V_T}} \qquad (4\text{-}7)$$

These results are plotted in Fig. 8, where it is seen that $V_{out,1}$ gives an inverting output, while $V_{out,2}$ is non-inverting. It should be noted that the numerical values of V_{out} can be either positive or negative,

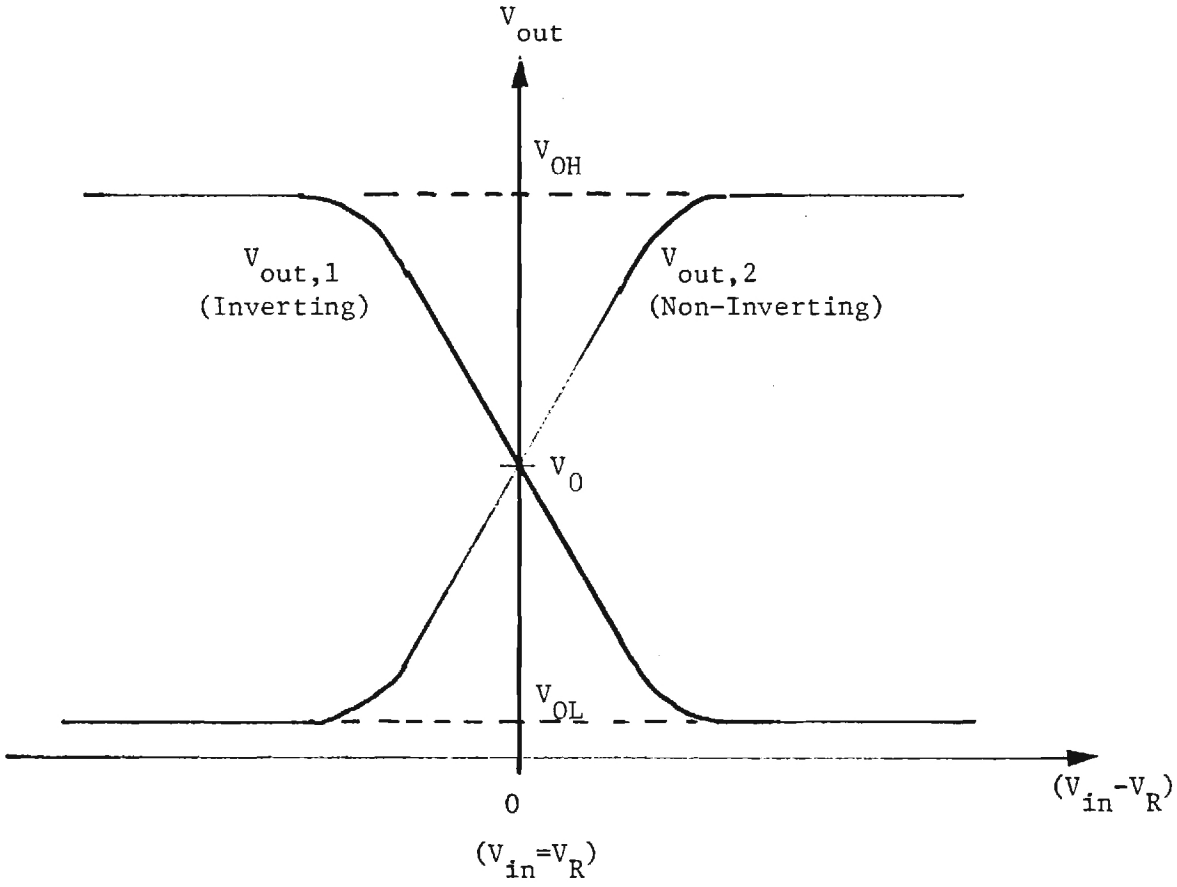


Figure 8

Basic ECL VTC Behavior

depending upon the values of V_{CC}, $-V_{EE}$ and I_{EE} .

The critical points of the VTC can be computed using straightforward techniques. First note that when $V_{in} = V_R$,

$$V_{out,1} = V_{out,2} = V_{CC} - \frac{1}{2}\alpha_F I_{EE} R_C \equiv V_0 \tag{4-8}$$

defines the output voltage. Next, suppose that $V_{in} >> V_R$. Then,

$$V_{out,1} \simeq V_{CC} - \alpha_F I_{EE} R_C \equiv V_{OL} \tag{4-9}$$

while

$$V_{out,2} \simeq V_{CC} \equiv V_{OH} \ . \tag{4-10}$$

The logic swing is thus given by

$$V_\ell \simeq \alpha_F I_{EE} R_C \tag{4-11}$$

and it is easily established that

$$V_0 = V_{CC} - \frac{1}{2} V_\ell \ . \tag{4-12}$$

To compute the critical input voltages, eqn. (4-11) is used to write the output voltages in the form

$$V_{out,\frac{1}{2}} = V_0 \pm \frac{1}{2} V_\ell \tanh \left[\frac{V_{in} - V_R}{2 V_T} \right] \quad . \tag{4-13}$$

Differentiating,

$$\frac{dV_{out,\frac{1}{2}}}{dV_{in}} = \mp \frac{1}{2} V_\ell \frac{1}{2V_T} \operatorname{sech}^2 \left[\frac{V_{in}-V_R}{2V_T} \right]$$

$$\equiv \mp 1 \tag{4-14}$$

where the last step is used to compute the 45° deflection points. Solving,

$$\cosh \left[\frac{V_{in} - V_R}{2V_T} \right] = \sqrt{\frac{V_\ell}{4V_T}} \quad . \tag{4-15}$$

Assuming that $(V_{in} - V_R) >> 2V_T$ then gives $\cosh(x) \simeq \frac{1}{2} e^x$ so

$$(V_{in} - V_T) \simeq V_T \ln\left(\frac{V_\ell}{V_T}\right) \tag{4-16}$$

with V_{in} being V_{IL} or V_{IH}. The input transition width is thus obtained as

$$TW \simeq 2 V_T \ln\left[\frac{V_\ell}{V_T}\right] \quad ; \tag{4-17}$$

it is easily seen that these critical voltages are dependent upon I_{EE} and R_C of the circuit.

As a final point in this discussion, it should be noted that the simplest practical realization for the current source is that where a

resistor R_{EE} is used as shown in Fig. 9. For this case, the emitter current I_{EE} is determined by

$$I_{EE} = \frac{V_R - V_{BE(on)} + V_{EE}}{R_{EE}} \quad . \tag{4-18}$$

The logic swing is then computed using

$$V_{OH} \simeq V_{CC}$$

$$V_{OL} \simeq V_{CC} - \frac{R_C}{R_{EE}} (V_R + V_{EE}) \tag{4-19}$$

so that

$$V_{\ell} \simeq \frac{R_C}{R_{EE}} (V_R + V_{EE}) \quad . \tag{4-20}$$

These demonstrate the importance of the power supply values V_{CC} and V_{EE} in setting the overall critical switching voltages.

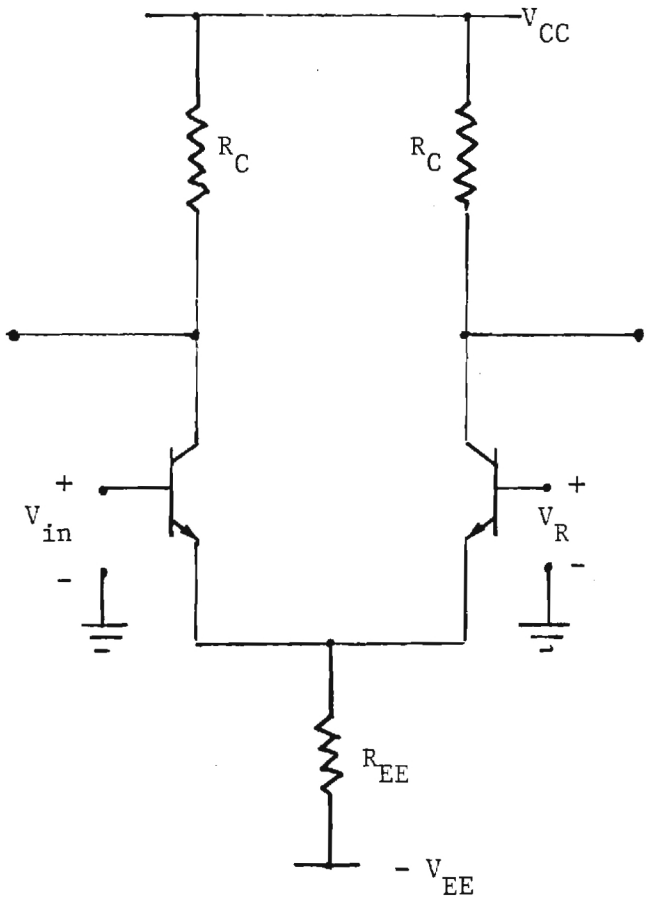


Figure 9

ECL Switch with Emitter Resistor

5. ECL OR/NOR Analysis

A good portion of the work described here centered around the behavior of an ECL OR/NOR gate as a means of obtaining information about the establishment of noise margins and voltage swings. Owing to this orientation, the analysis of the ECL OR/NOR gate is of great interest.

A general N-input gate is illustrated in Fig. 10. The OR/NOR function has been obtained from the basic inverter/amplifier by simply parallelling N transistors Q1, Q2, ..., QN. The bias is established by transistors QA and QB, while Q0 is used to input the reference voltage V_R. It is assumed that all transistors are identical.

The most general case which can be analyzed is that where m of the inputs have high voltages V_{OH} applied to them, while the remaining (N-m) inputs have V_{OL} logic 0 levels. Applying KCL at the common emitter node gives

$$I_{EE} = mI_{SE}e^{(V_{OH}-V_E)/V_T} + (N-m)I_{SE}e^{(V_{OL}-V_E)/V_T} + I_{SE}\, e^{(V_R-V_E)/V_T} \qquad (5\text{-}1)$$

where V_E is the voltage at the node. Since the second term represents the current through the transistors which are off, it is ignored and set equal to zero. The collector currents are thus found to be

$$I_{CR} = \alpha_F\, I_{SE}\, e^{(V_R-V_E)/V_T} \qquad (5\text{-}2)$$

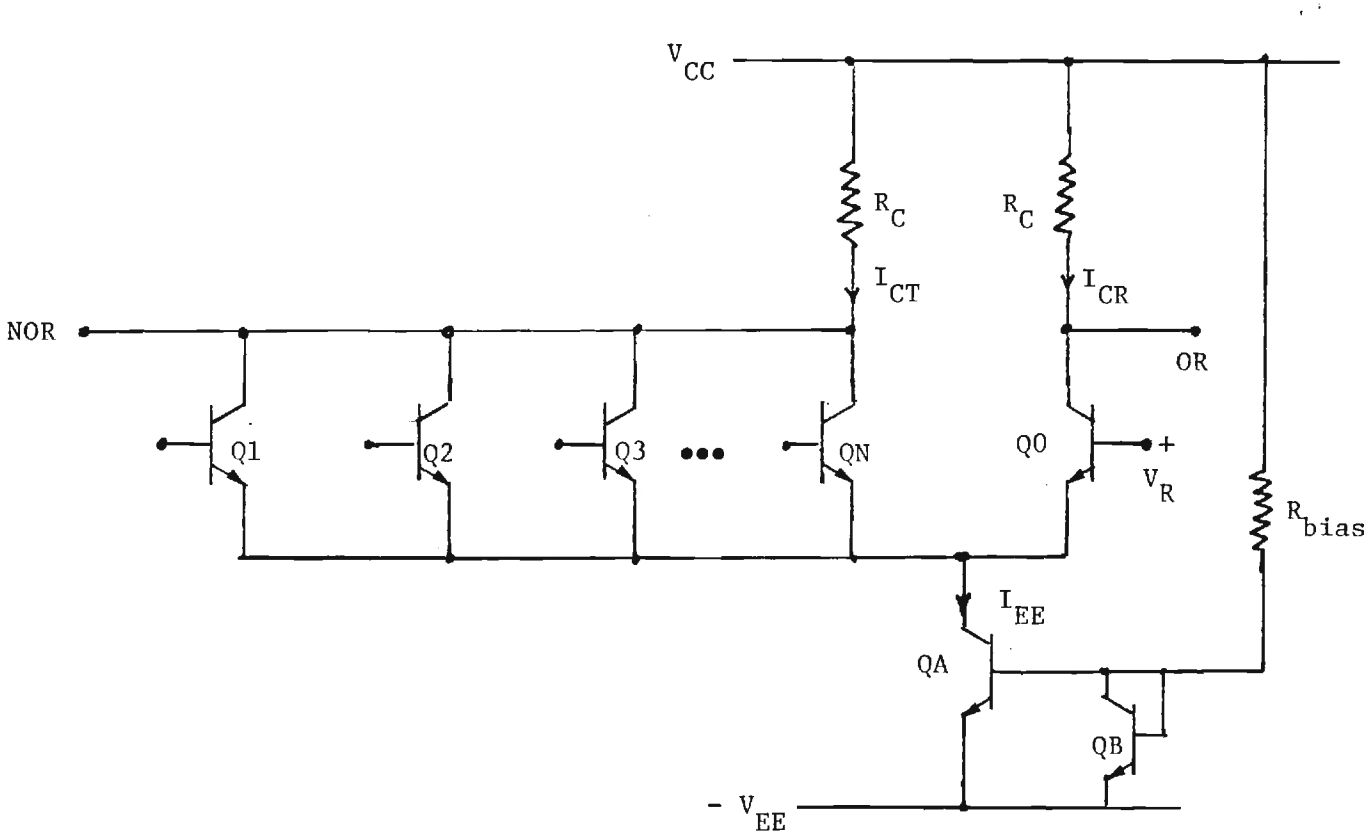


Figure 10

Internal Structure of ECL OR/NOR

and

$$I_{CT} \simeq \alpha_F I_{EE} - \alpha_F I_{SE} e^{(V_R - V_E)/V_T}$$

$$\simeq \alpha_F m I_{SE} e^{(V_{OH} - V_E)/V_T} \qquad (5\text{-}3)$$

so that the output node voltages are obtained as

$$V_{NOR} = V_{CC} - I_{CT} R_C$$

$$V_{OR} = V_{CC} - I_{CR} R_C \quad . \qquad (5\text{-}4)$$

The VTC may be computed by assuming that m input are being switched simultaneously. With the input voltage equal to V_{in}, the analysis gives collector currents of

$$I_{CT} = \frac{\alpha_F I_{EE}}{1 + \frac{1}{m} e^{-(V_{in} - V_R)/V_T}}$$

$$I_{CR} = \frac{\alpha_F I_{EE}}{1 + m e^{(V_{in} - V_R)/V_T}} \quad . \qquad (5\text{-}5)$$

Note that the case m=1 degenerates to the expressions found in the previous section. These currents may be directly substituted into the voltage equations (5-4) which then gives the characteristic transfer equations. Figure 11 provides an example of how the VTC is modified depending upon the number of inputs which are switched. The critical

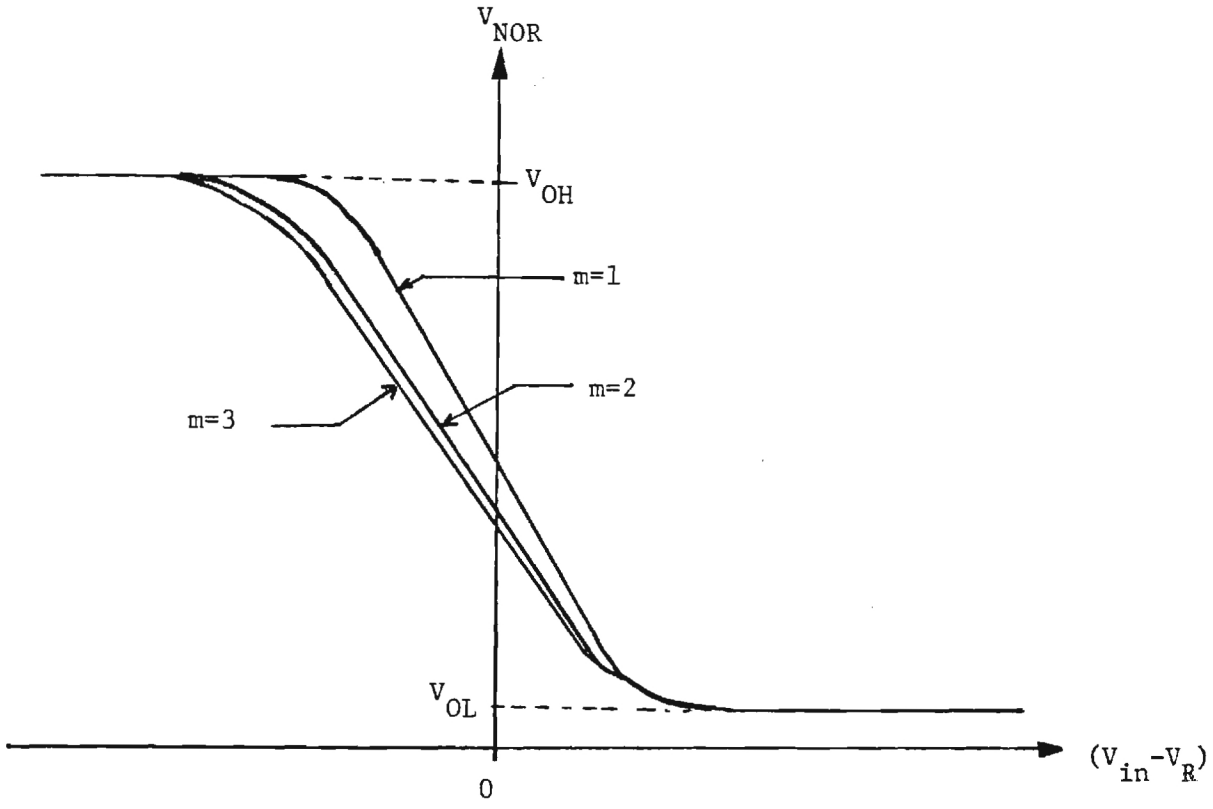


Figure 11

ECL OR/NOR VTC with
m Inputs Switched

VTC voltage levels are computed as before. The logic swing is found to be

$$V_\ell = \alpha_F I_{EE} R_C$$

$$= \frac{\alpha_{FA}\alpha_F}{(2 - \alpha_{FA})} \frac{R_C}{R_{bias}} [V_{CC} - V_{BE(on),B}] \qquad (5\text{-}6)$$

where α_{FA} is the forward current gain of the current source transistor QA. The noise margins are given by

$$NM_L = \frac{1}{2} V_\ell - V_T \ln \left[\frac{mV_\ell}{V_T} \right]$$

$$NM_H = \frac{1}{2} V_\ell - V_T \ln \left[\frac{V_\ell}{mV_T} \right] \qquad (5\text{-}7)$$

which summarizes the theoretical behavior of the switching characteristics.

A final important point to note is the fact that the output nodes shown in Fig. 10 are usually connected to driver stages at some point in the overall logic formation system. A typical emitter-follower driver is illustrated in Fig. 12. This circuit requires that the logic swing satisfy the constraint

$$V_\ell \leq V_{BE(out)} \qquad (5\text{-}8)$$

in order to keep the input transistors out of saturation when $V_{NOR}=V_{OL}$. The non-saturation requirement thus establishes a design criteria with regards to the overall circuit configuration.

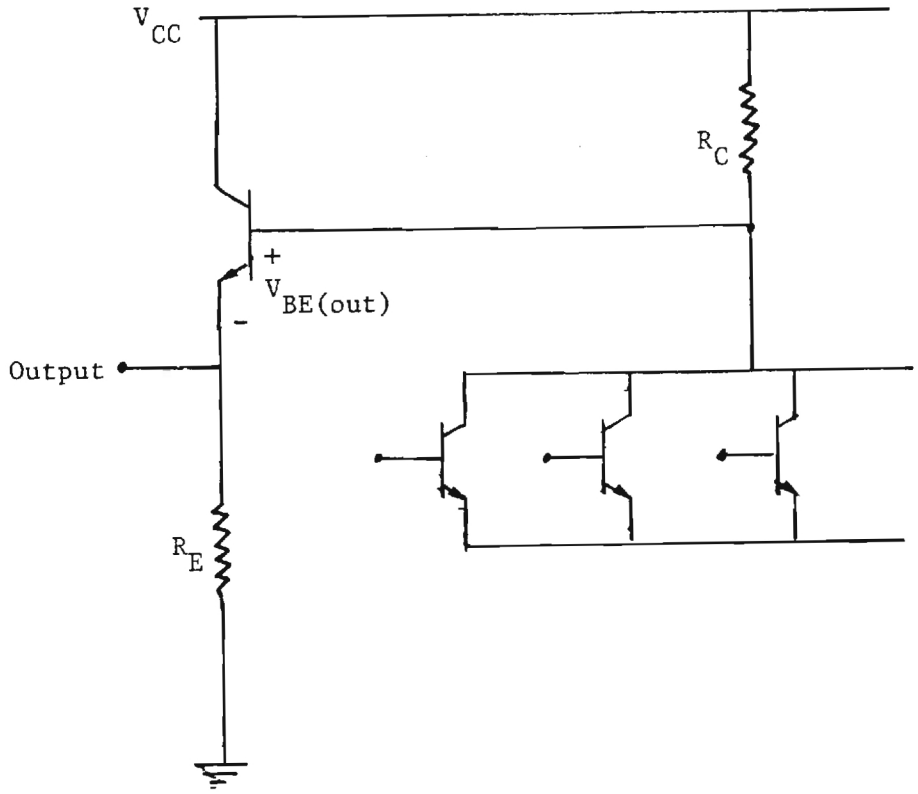


Figure 12

Emitter-Follower Output
Stage for ECL

6. SPICE ECL Analysis

A major objective of the work described here was to isolate the most important device and circuit parameters which structure the overall switching characteristics of an ECL OR/NOR gate. This phase of the project was performed in a "brute force" manner by using the circuit simulation program SPICE extensively. The approach was simply to vary one parameter at a time as a means of obtaining any overall trends which could be established. As will be seen in the results presented in this section, it was possible to isolate and classify the parameters which lead to the formation of voltage noise margins and the other critical VTC paramters. The information will be presented in both graphical and tabular form.

The basic circuit used in the SPICE analysis is shown in Fig. 13 where it is noted that $V_{CC} = 1.7$ [V] and $V_{EE} = 0$ [V] have been chosen arbitrarily. The circuit is a bit smplistic in that it uses balanced collector resistors of value 1.2 [kΩ]. The reference voltage V_R has been chosen to be 1.4 [V]. Assuming a $V_{BE(on)}$ value of 0.7 [V] gives a nominal emitter current of

$$I_{EE} \simeq 2 \frac{1.4 - 0.7}{1400} = 1.0 \text{ [mA]} \qquad (6\text{-}1)$$

when $V_{in} = V_R$. Although this simple bias scheme does not provide for a stable I_{EE} value, the circuit was chosen because it would readily allow for extraction of the important dependences.

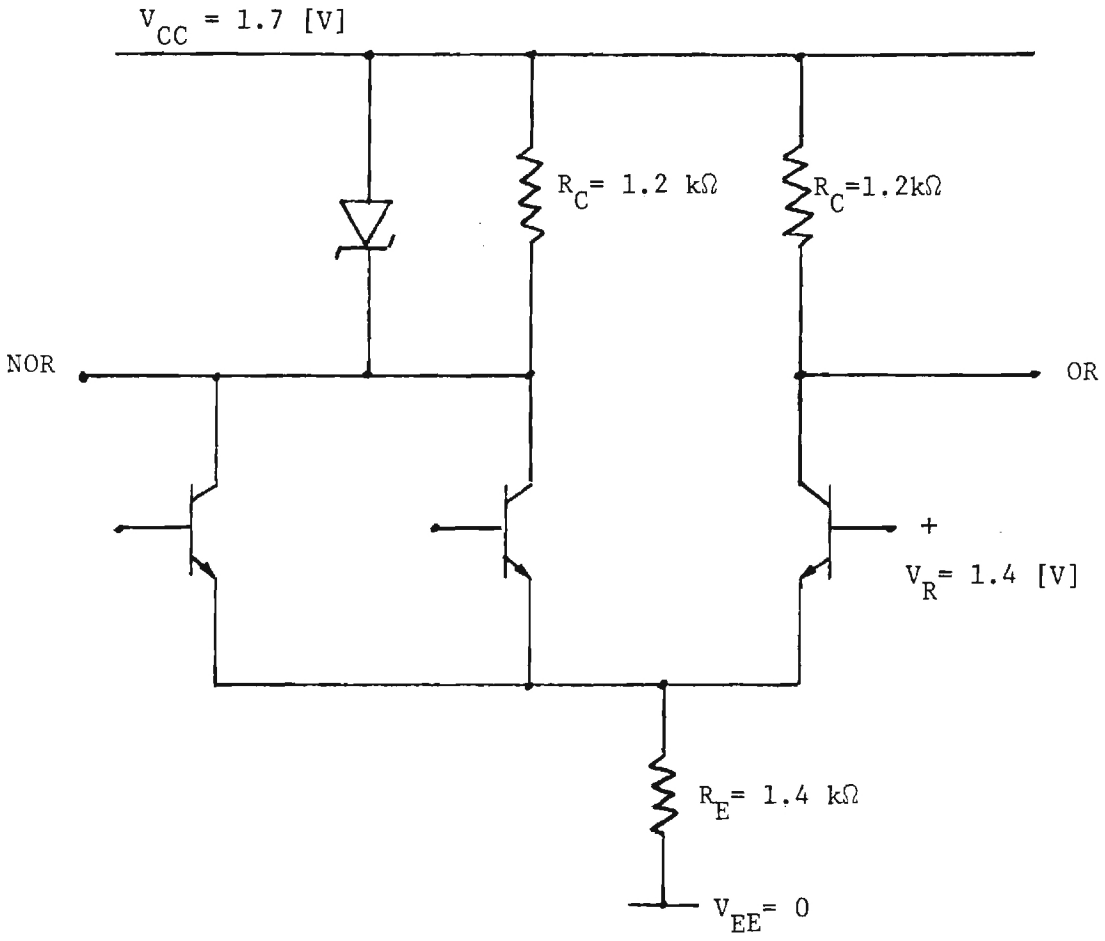


Figure 13

2-Input ECL OR/NOR Gate
used in SPICE Analysis

Modified Gummel-Poon SPICE Parameters
for Bipolar Transistors

Symbol	Name	Default	Units
I_S	Transport Saturation Current	1×10^{-16}	A
β_F	Ideal Maximum Forward Gain	100	-
η_F	Forward Current Emission Coefficient	1,0	-
V_{AF}	Forward Early Voltage	∞	V
I_{SE}	Base-Emitter Saturation Leakage	0	A
η_E	Base-Emitter Emission Coefficient	1,5	-
β_R	Maximum Reverse Current Gain	1	-
η_R	Reverse Emission Coefficient	1	-
V_{AR}	Reverse Early Voltage	∞	V
I_{KR}	Corner for Reverse Beta Roll-Off	∞	A
I_{SC}	Base-Collector Saturation Current	0	A
η_C	Base-Collector Emission Coefficient	2	-
r_B	Base Resistance at Zero Bias	100	Ω
I_{RB}	Current for $r_B/2$	∞	A
r_{BM}	Minimum Base Resistance (High Current)	r_B	Ω
r_E	Emitter Resistance	0	Ω
r_C	Collector Resistance	0	Ω
C_{jE}	B-E Zero-Bias Depletion Capacitance	0	F
V_{jE}	Base-Emitter Built-in Voltage	0,75	V
m_{jE}	B-E Junction Exponential Factor	0,33	V
T_F	Forward Transit Time	0	s
X_{TF}	Bias Dependent Factor for T_F	0	-
V_{TF}	Voltage for V_{BC} T_F Dependence	∞	V
I_{TF}	High Current T_F Factor	0	A
P_{TF}	Phase Excess for T_F	0	Deg.
C_{jC}	B-C Zero- Bias Depletion Capacitance	0	F
V_{jC}	B-C Built-in Voltage	0,75	V
m_{jC}	B-C Junction Exponential Factor	0,33	-
XC_{jC}	Fraction of C_{jC} on Base Node	1	0

Table 1

Symbol	Name	Default	Units
T_R	Reverse Transit Time	0	s
C_{jS}	Zero-Bias C-Substrate Capacitance	0	F
V_{jS}	Substrate-Junction Built-In Voltage	0.75	V
m_{jS}	Substrate-Junction Exponential Factor	0	-
X_{TB}	Forward and Reverse Beta Temperature Exponent	0	-
E_g	Energy Gap	1.11	eV
X_{TI}	Temperature Exponent for I_S	3	-
K_F	Flicker-Noise Coefficient	0	-
A_F	Flicker-Noise Exponent	1	-
F_C	Forward-Bias Depletion Capacitance Factor	0.5	-
I_{KF}	Forward Beta High-Current Roll-Off	∞	A

Table 1

Parameters Used in Level 2
SPICE Transistor Modelling

The SPICE simulations were run at 3 different temperatures (10°C, 27°C and 85°C) for each parameter studied. Each variation resulted in values for V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_{ℓ}, NM_H, NM_L and TW. To insure as much accuracy as possible, the SPICE Level 2 bipolar transistor model was used. This is basically a modified Gummel-Poon charge-control formulation which allows for input changes in addition to non-ideality factors and parasitics. The SPICE parameters are listed in Table 1 for future reference. Unless otherwise noted, a parameter was left to its default value.

The first set of variations which are provided here are those which depend upon the value of the Transport Saturation Current I_S. These are shown in Figs. 14 (a), (b) and (c) representing the three temperature values. In Fig. 14(a), it is seen that V_{OL}, V_{IL} and NM_L exhibit the greatest variations. The room temperature plots(27°C) in Fig. 14(b) show similar dependences, with a noticeable change taking place in the input critical voltages V_{IL} and V_{IH}. The high temperature plots in Figs. 14(c) show that the changes have transferred over to the input voltages, with only minor perturbations to V_{OL} and V_{OH}. This set of graphs shows that the circuit switching characteristics are quite dependent upon I_S and T.

The next set of plots in Figs, 15 (a), (b) and (c) illustrate the important voltage quantities when the base-emitter built-in voltage is changed. It is easily seen that there is virtually no effect of the curves on this quantity. Thus, V_{jE} is eliminated as a source of noise margin variations.

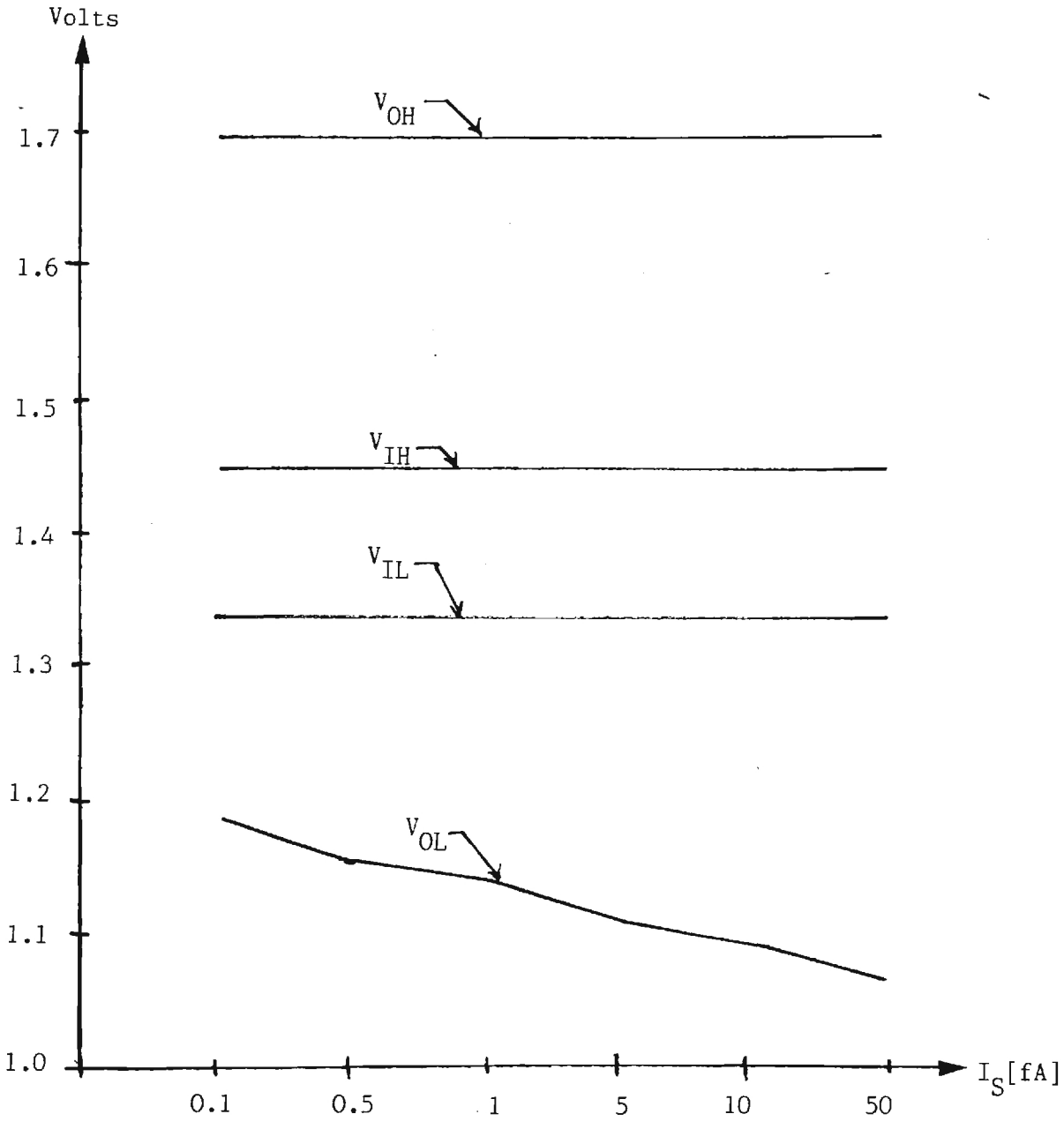


Fig. 14(a)
T = 10°C

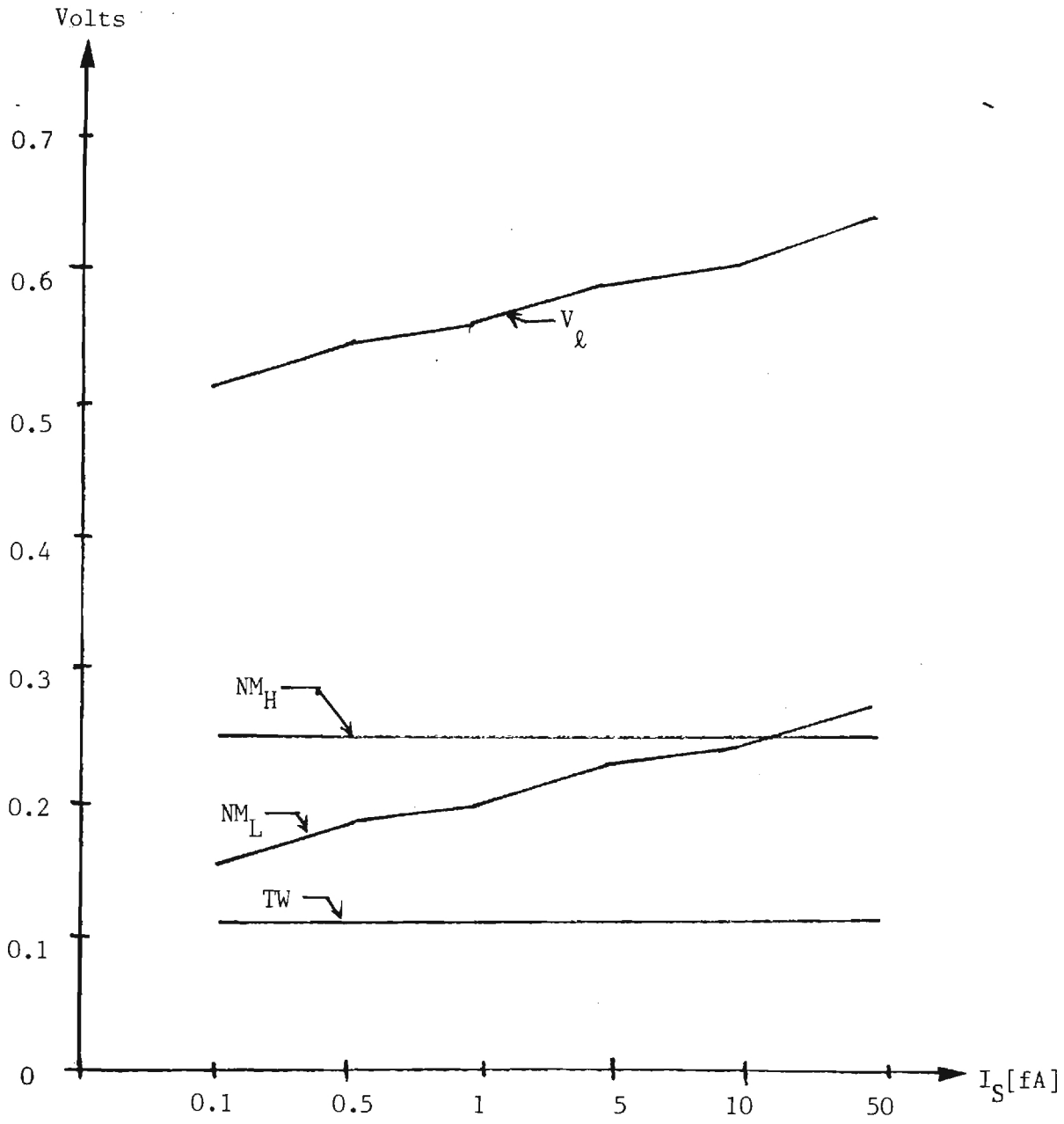


Fig. 14(a) Continued
T = 10°C

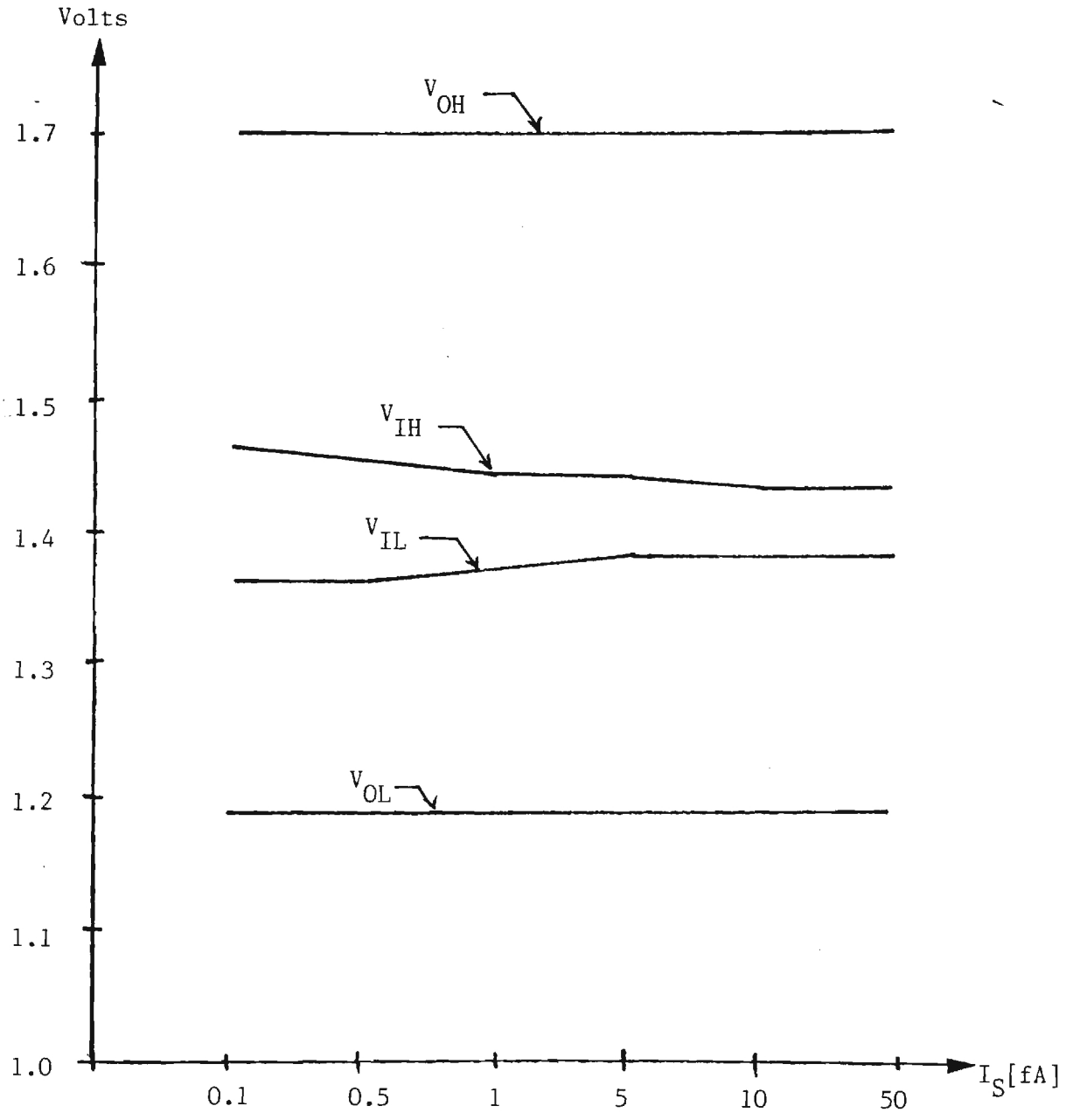


Fig. 14(b)
T = 27°C

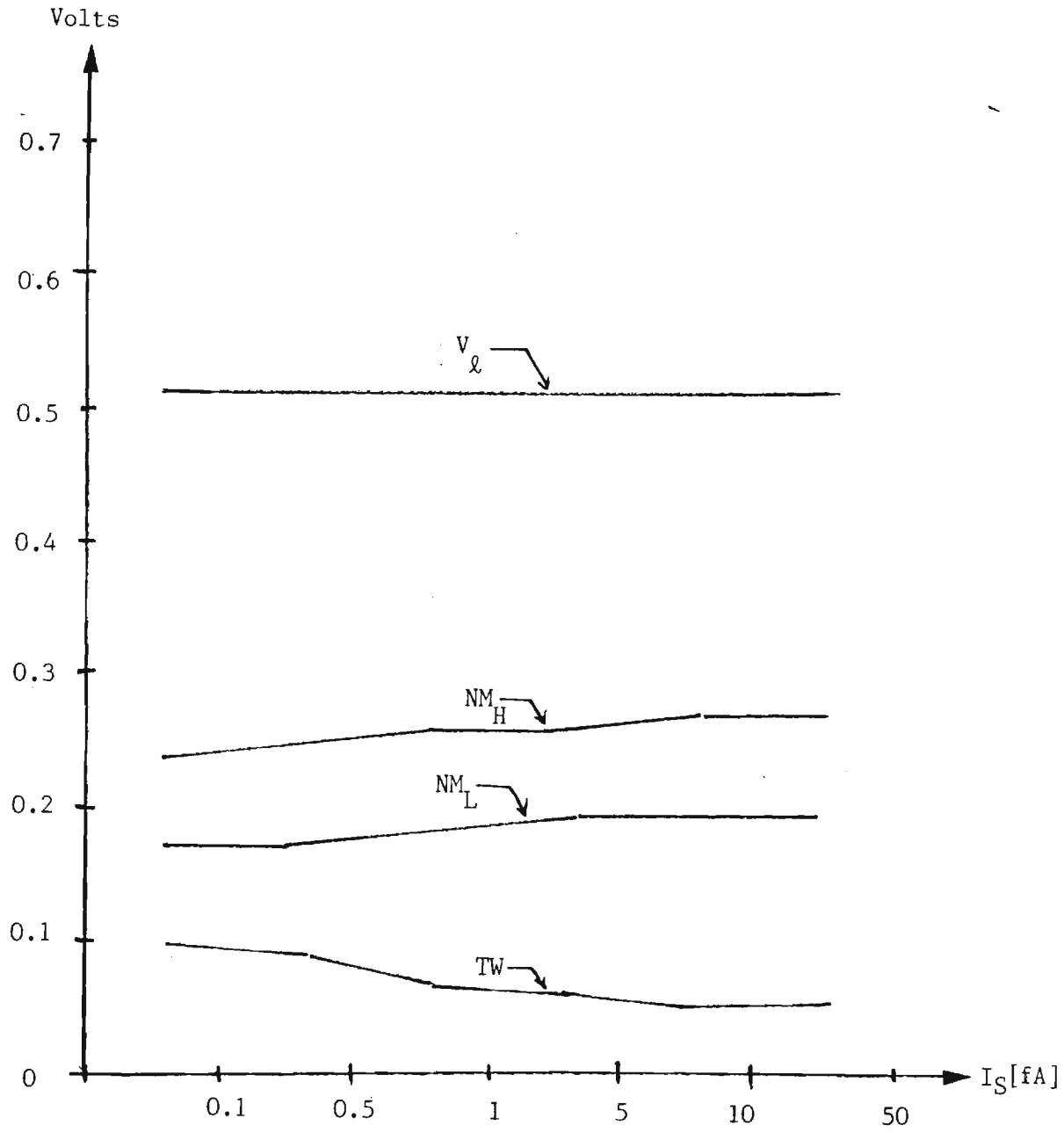


Fig. 14(b)-Continued
T = 27°C

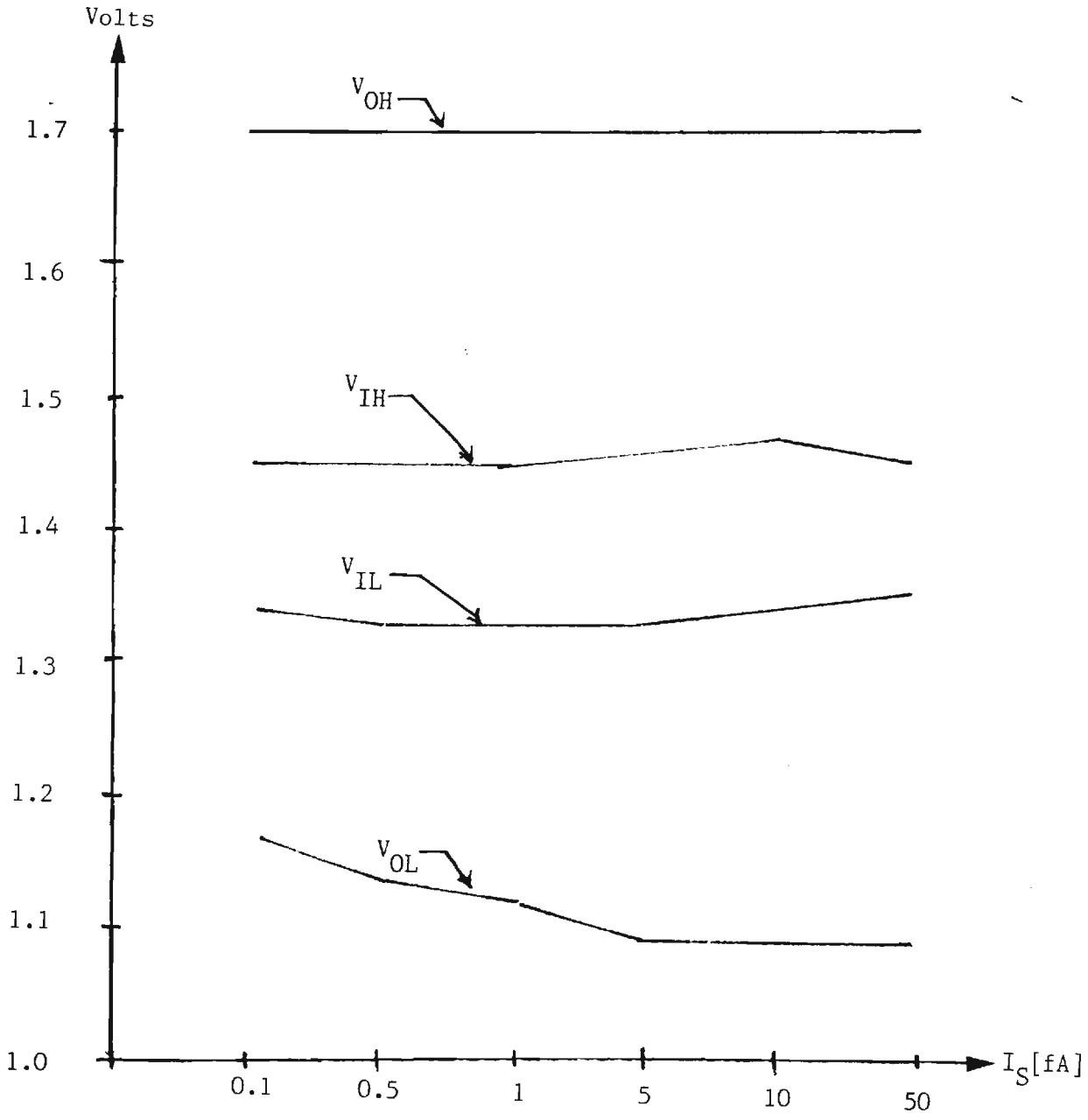


Fig. 14(c)
T = 85°C

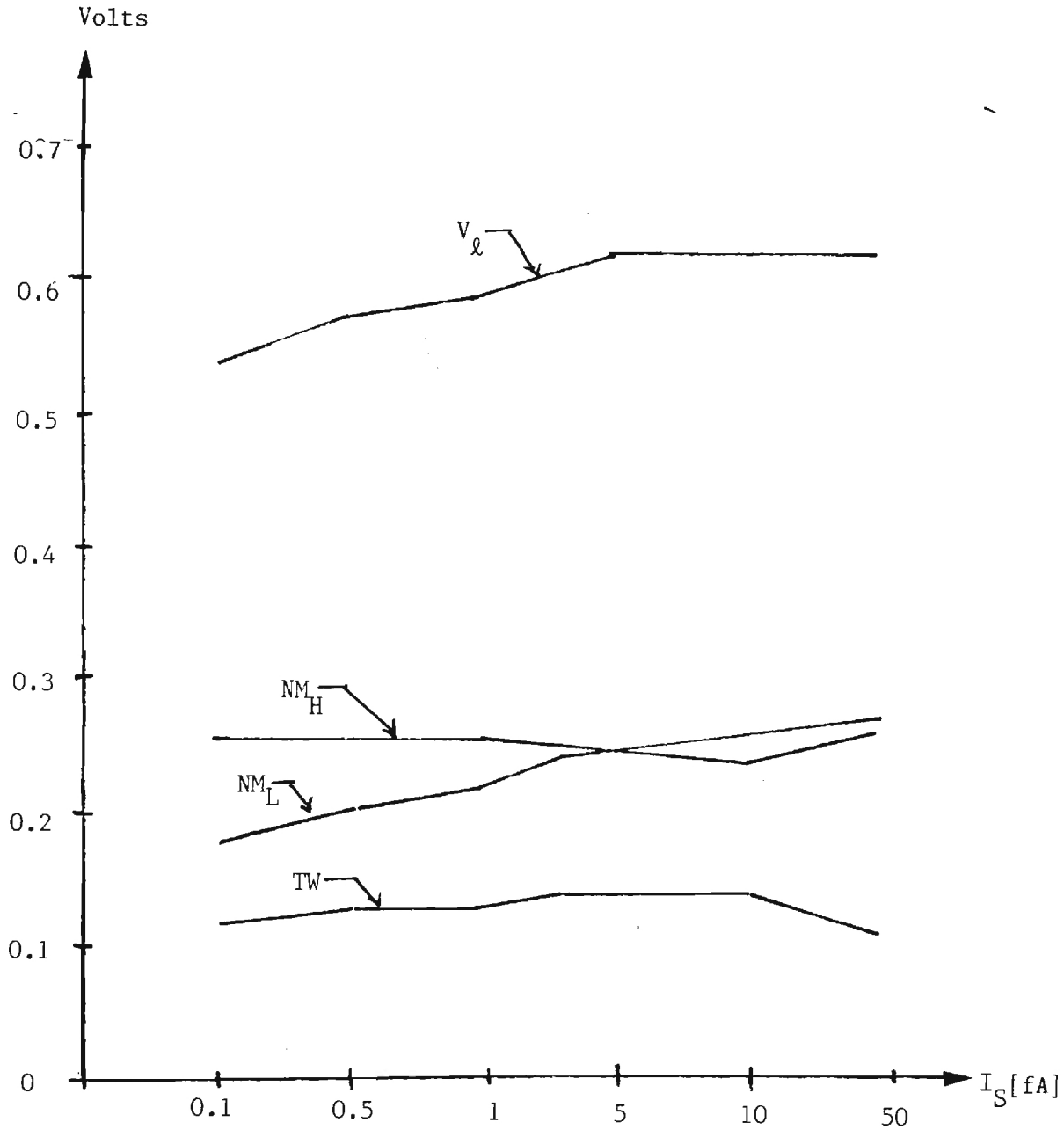


Fig. 14(c)-Continued
T = 85°C

Figure 14
VTC Dependence on I_S

V_{jE}=0.7 [V], r_B=150 [Ω], r_c= 100 [Ω], β_F= 80
η_F= 1.008 $I_{KF} = 2^c \times 10^{-3}$

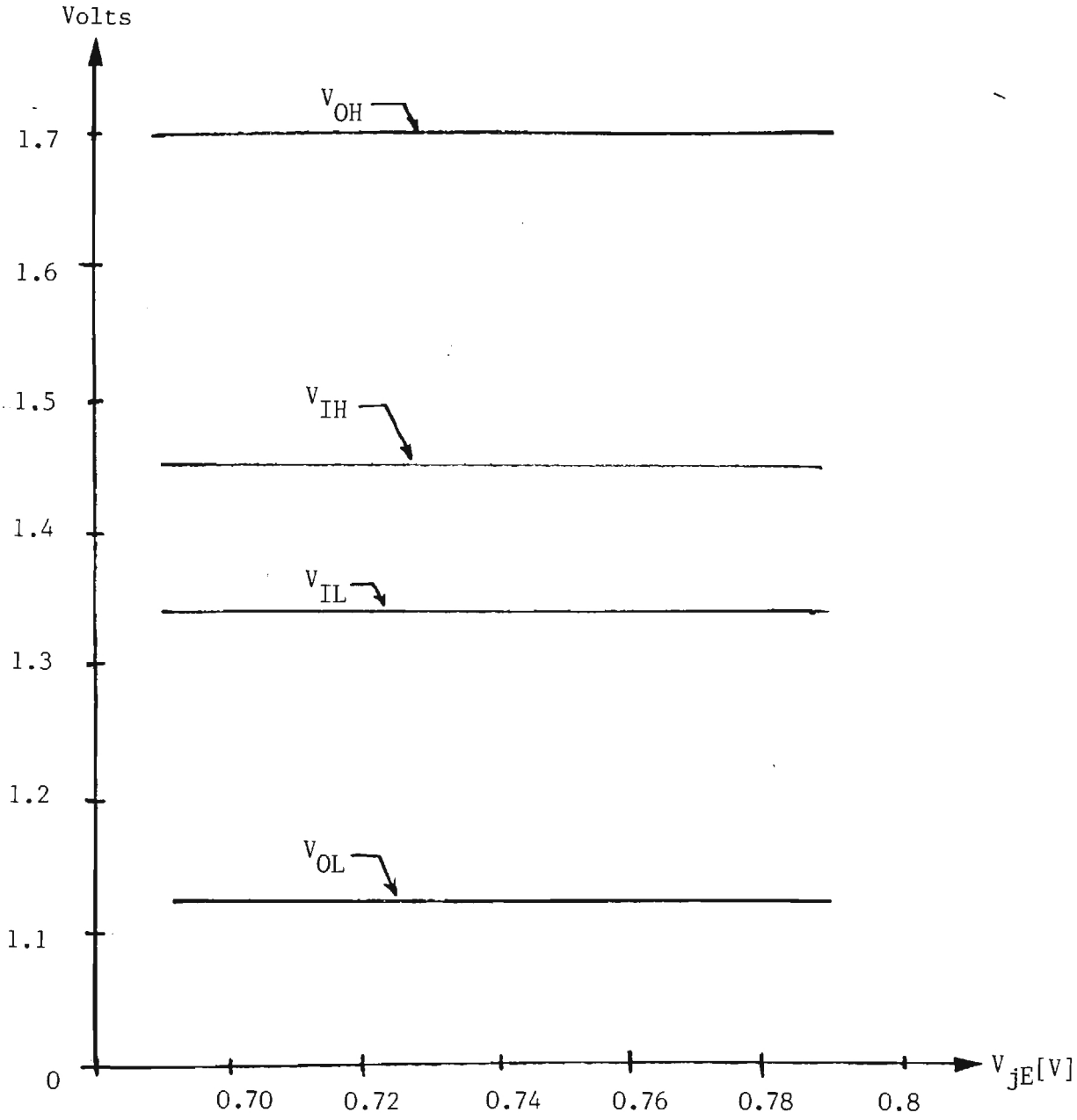

Volts
1.7
1.6
1.5
1.4
1.3
1.2
1.1
0
V_{OH}
V_{IH}
V_{IL}
V_{OL}
0.70
0.72
0.74
0.76
0.78
0.8
V_{jE}[V]

Fig. 15(a)

T= 10°C

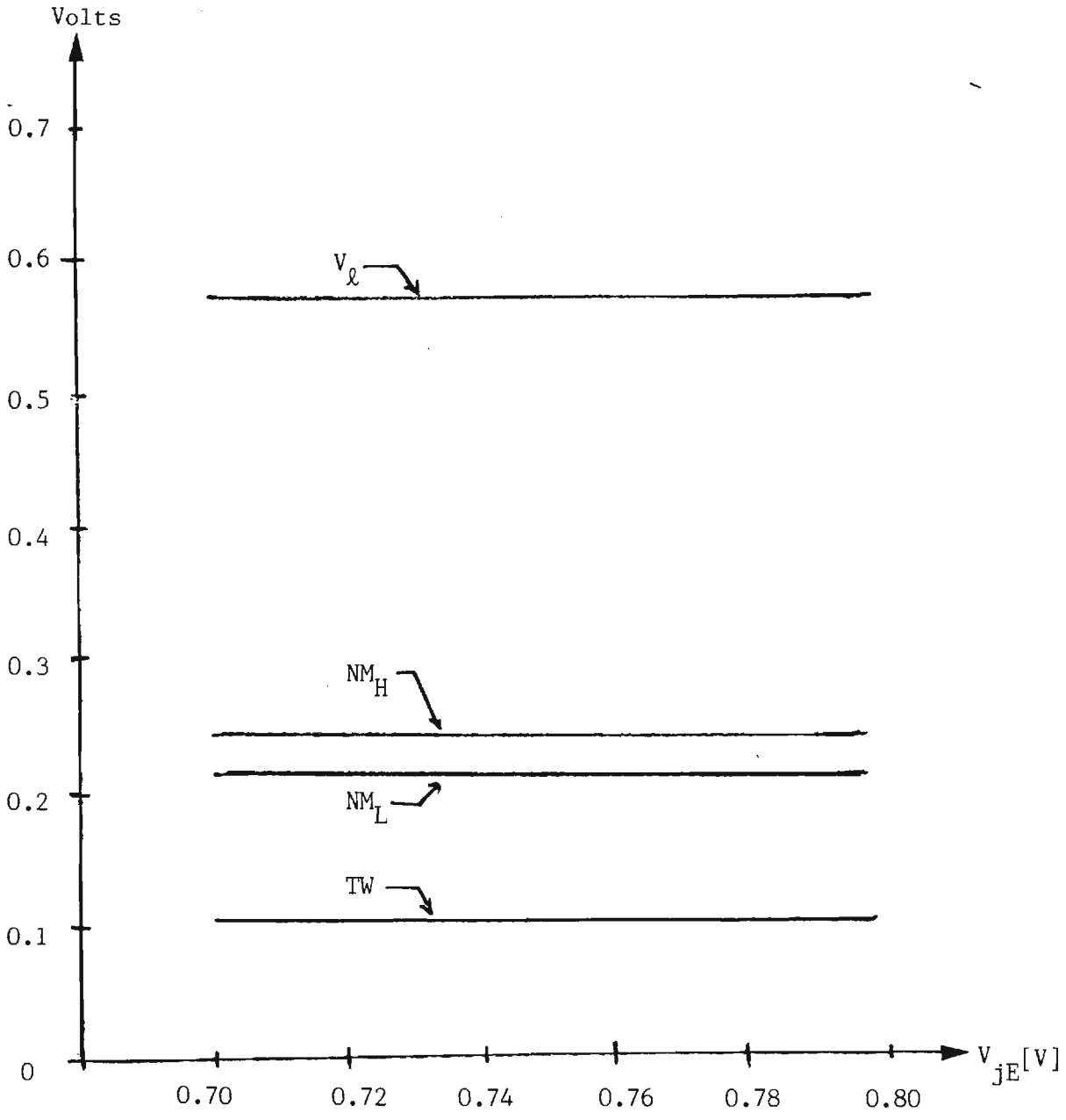


Fig. 15(a)-Continued
T = 10°C

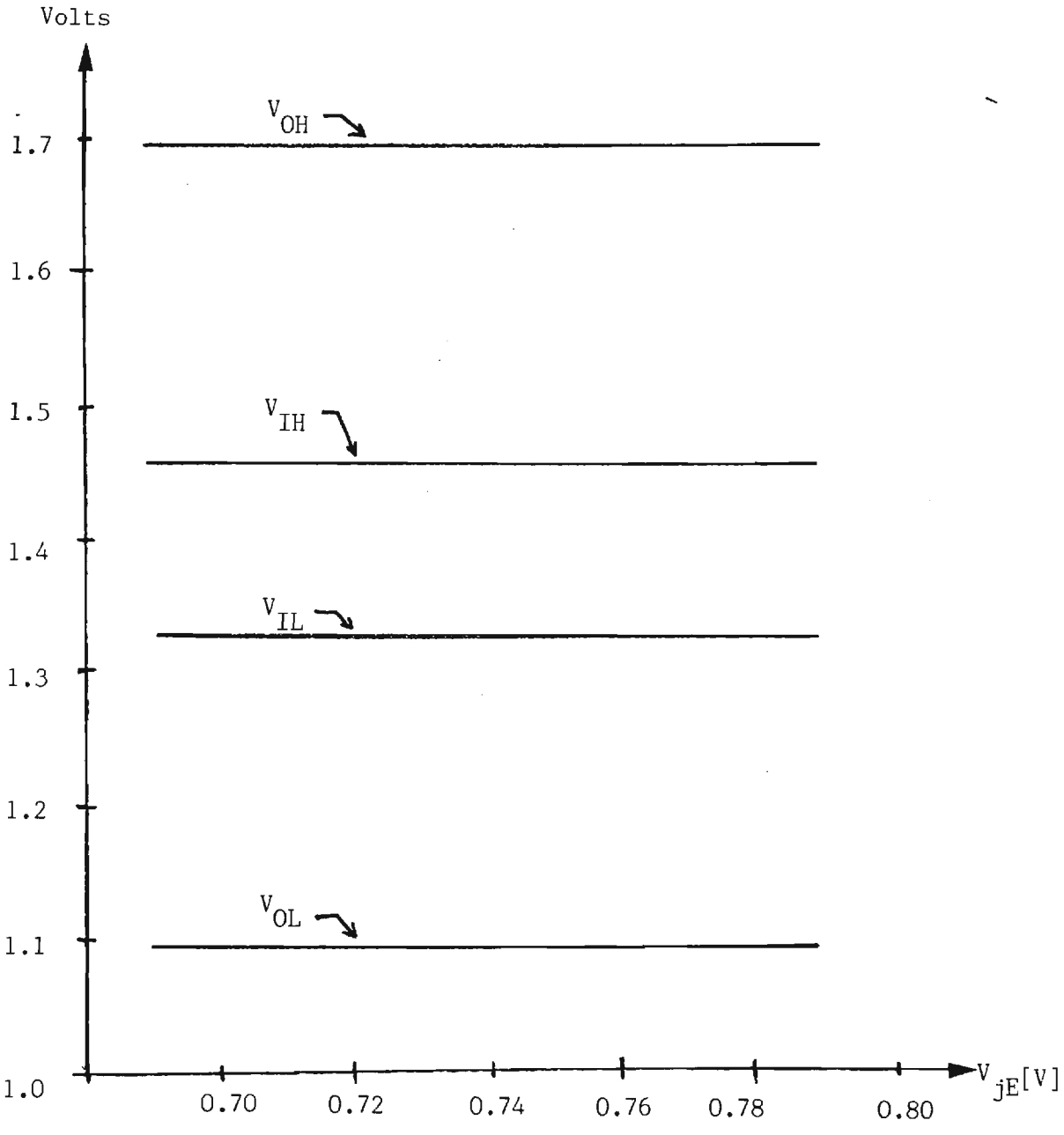

Volts
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
V_{OH}
V_{IH}
V_{IL}
V_{OL}
0.70
0.72
0.74
0.76
0.78
0.80
V_{jE}[V]

Fig. 15(b)
T = 27°C

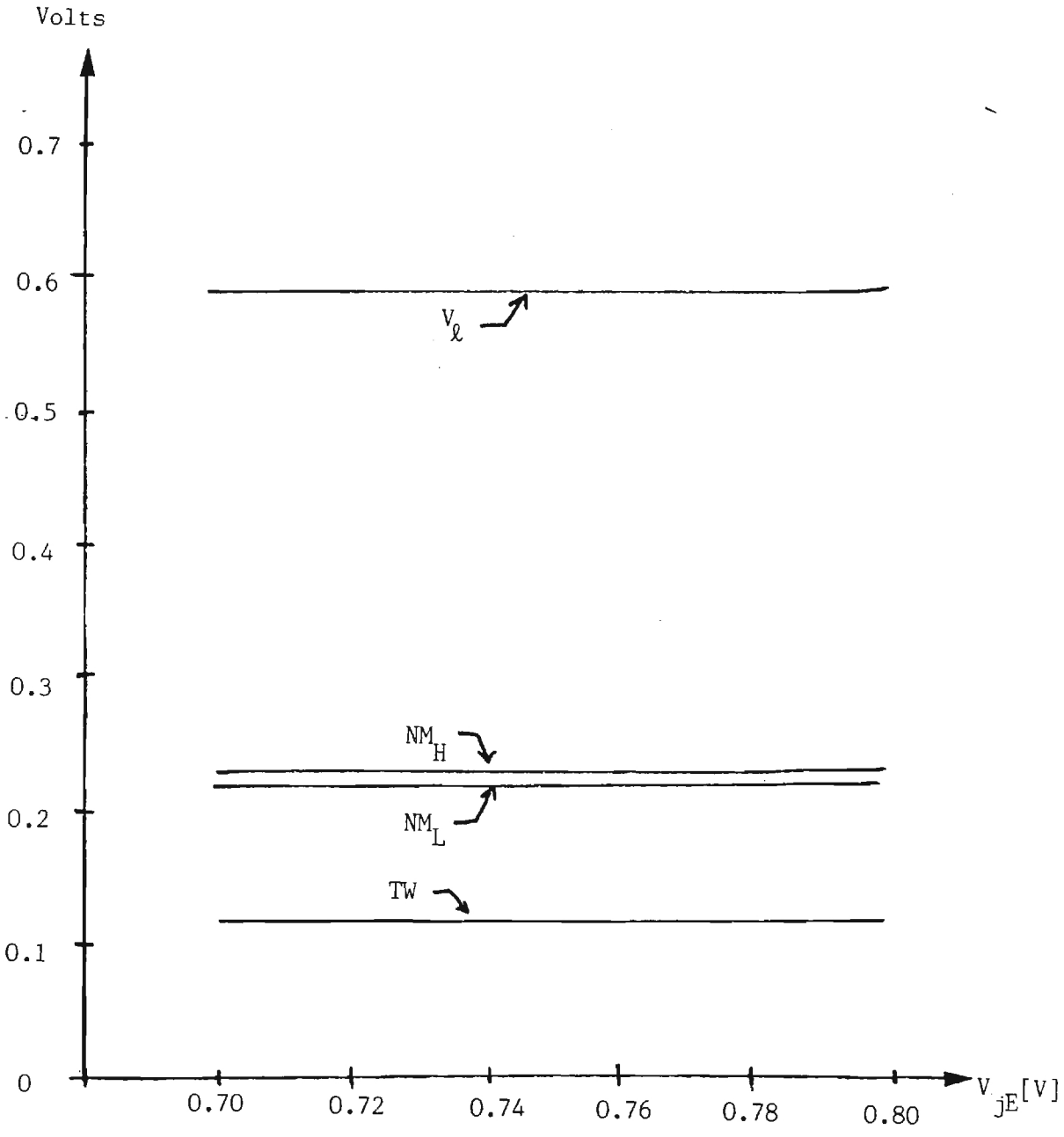


Fig. 15(b)- Continued
T= 27°C

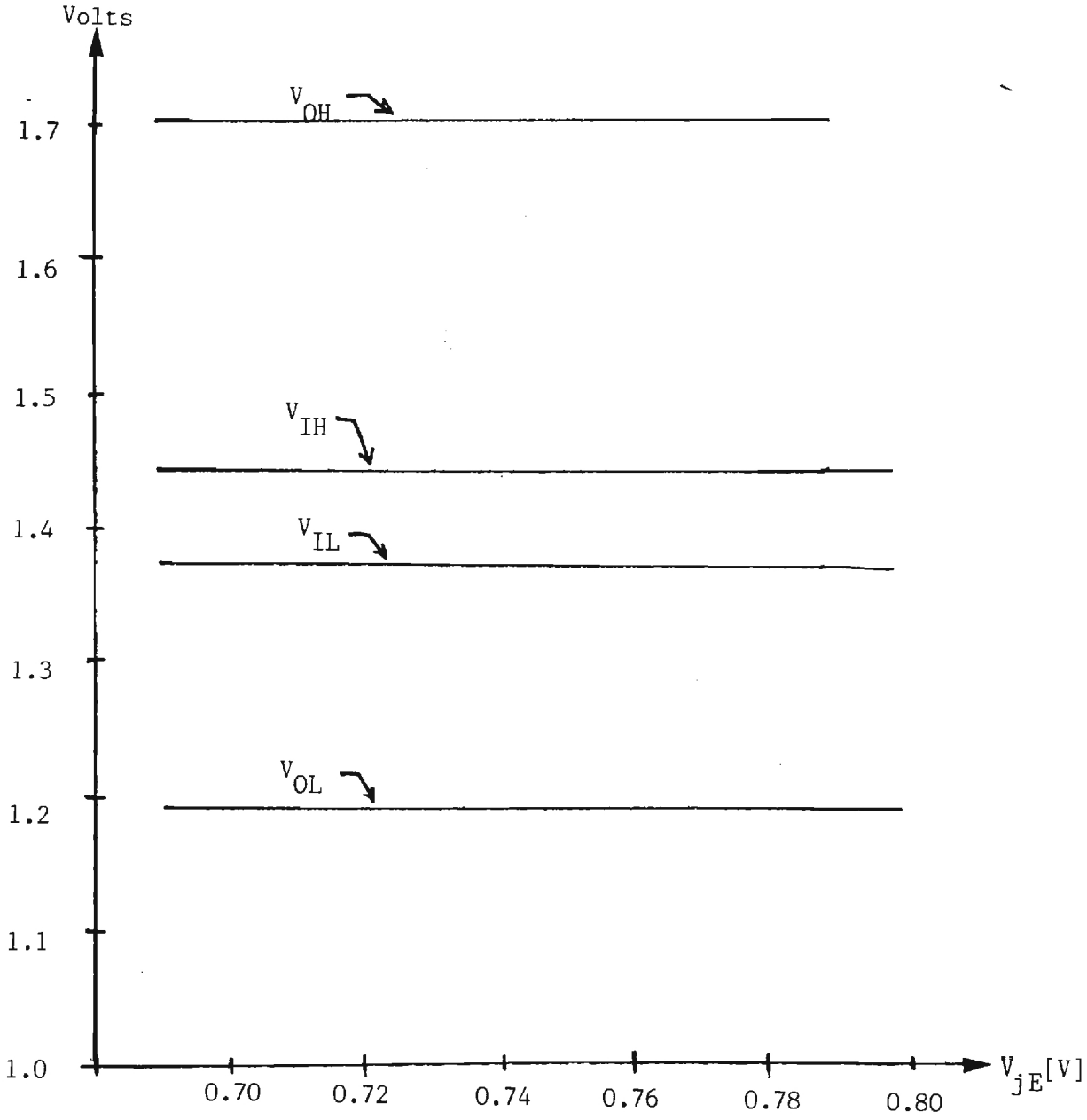

Volts
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
V_{OH}
V_{IH}
V_{IL}
V_{OL}
0.70
0.72
0.74
0.76
0.78
0.80
V_{jE}[V]

Fig. 15(c)
T = 85°C

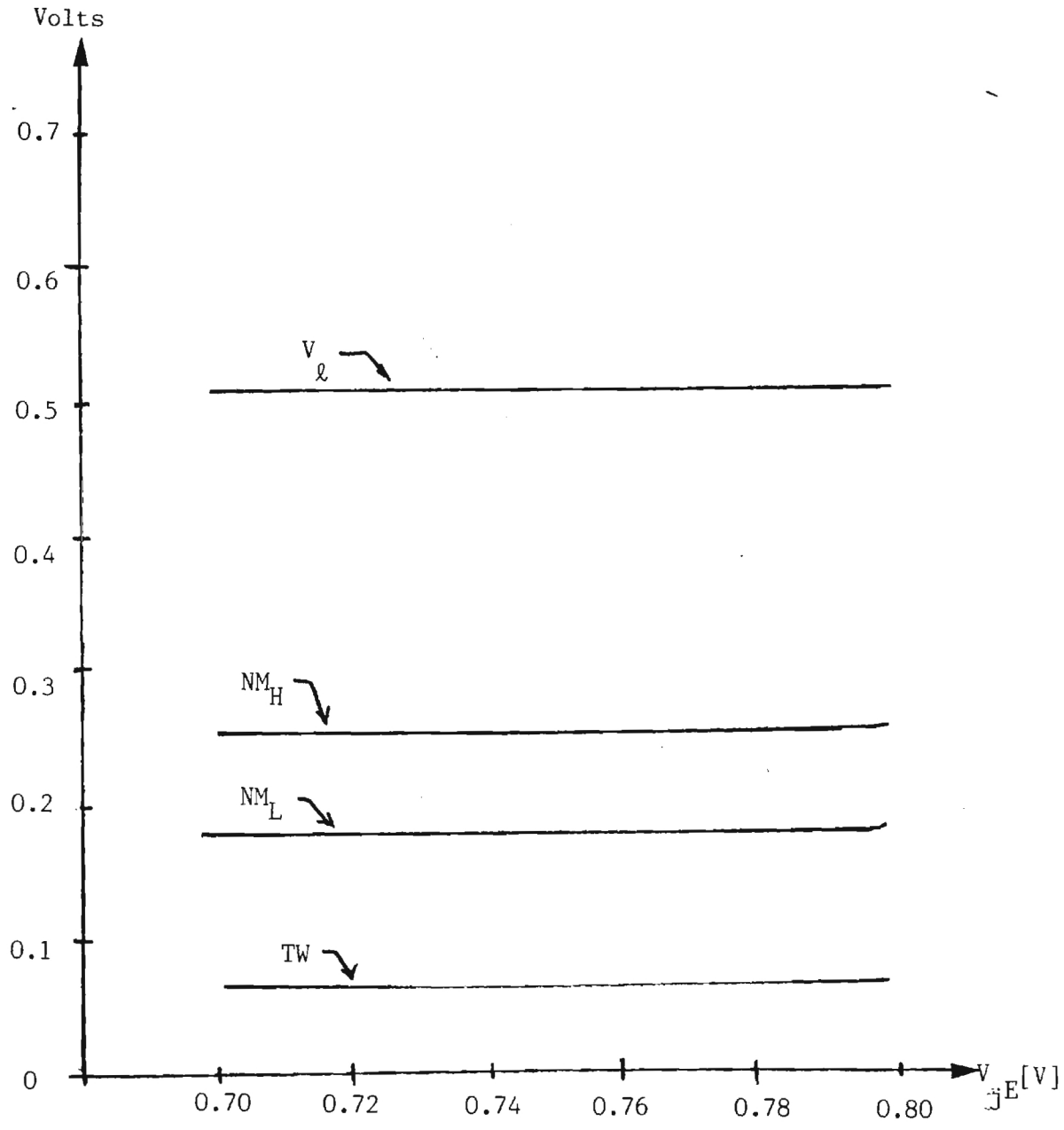


Fig. 15(c)-Continued
T = 85°C

Figure 15

VTC Dependence on V_{jE}

β_F=80, r_B=150[Ω], r_C=100 [Ω], I_S = 2.93 [fA], η_F=1
I_{KF}= 2 x 10^{-3}

The circuit was analyzed for variations due to changes in the forward current gain β_F with the results shown in Fig. 16(a), (b) and (c). It is obvious that the circuit is relatively insensitive to the exact value of β_F used in the circuit calculations.

Figures 17(a), (b) and (c) represent the circuit performance as a function of the parasitic base resistance r_B. The parameters for the VTC characterization do not change much over the range of values tested. Figure 18 gives the toom temperature behavior when the parasitic collector resistance r_C is varied. The curves for this case are also relatively invariant. These graphs thus allow the elimination of the three parameters β_F, r_B and r_C as being important in variations of the VTC critical voltages and the circuit noise margins.

Other parameters were tested and eliminated as a source of possible VTC variations. These include the Early voltages V_{AF} and V_{AR}, and also I_{KR}. The data which led to these conclusions is not presented here since it was judged irrelevant.

The power supply value V_{CC} was also varied in a series of SPICE simulations. The lowest level studied numerically was V_{CC} = 1.2 [V] which indicated a best-case logic swing of $V_\ell \simeq 450$ [mV] with standard values for the device parameters. The level of V_{CC} = 1.7 [V] was chosen for most of the work since it tended to optimize the numerical results in that the VTC variations were large enough to be obvious on a run-to-run basis. It is noted at this point that Section 7.5 deals with the question of the minimum V_{CC} which can be handled in the circuit.

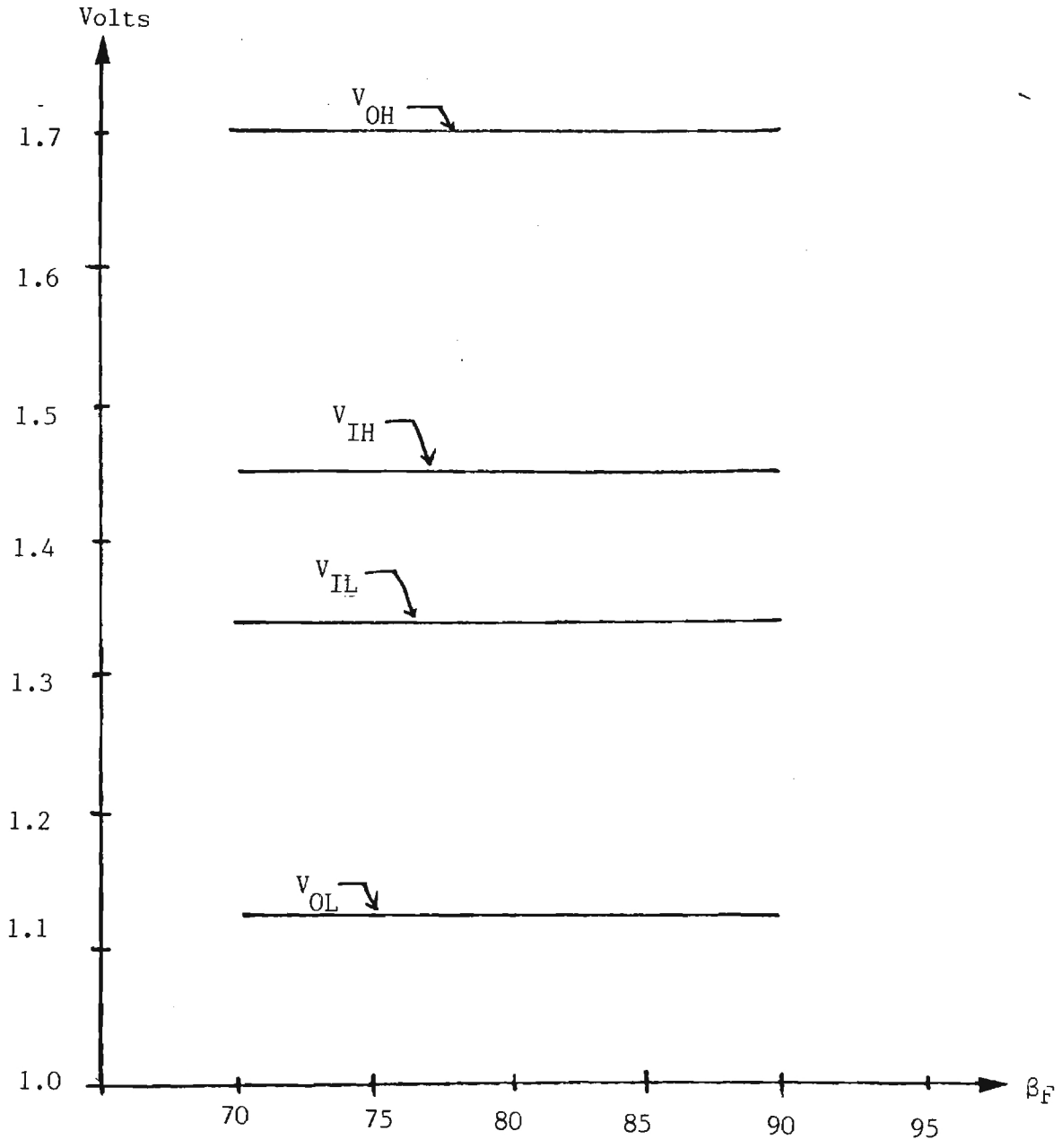

Volts
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
V_{OH}
V_{IH}
V_{IL}
V_{OL}
70
75
80
85
90
95
β_F

Fig. 16(a)
T=10°C

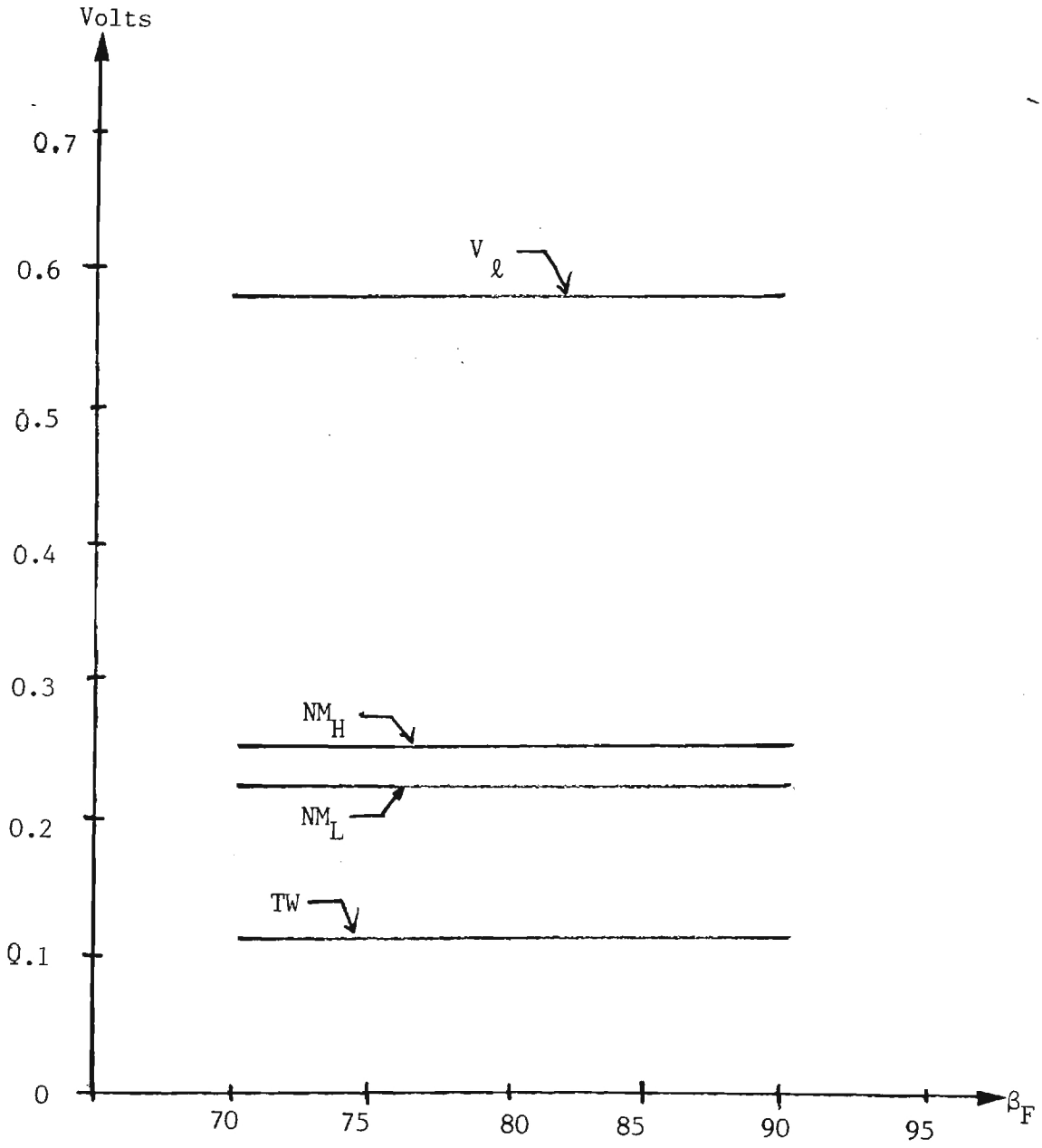


Fig. 16(a)-Continued
T = 10°C

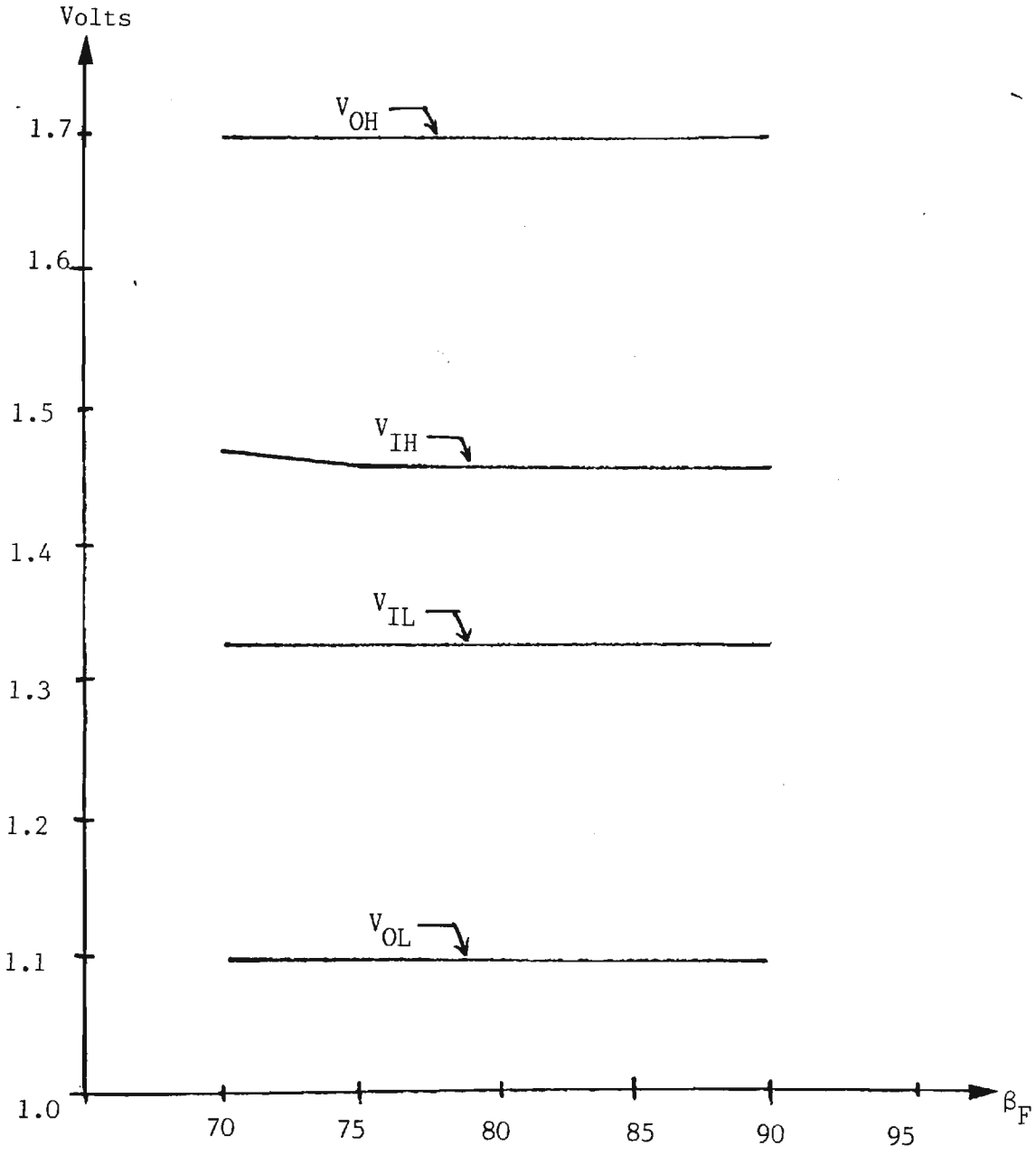

Volts
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
V_{OH}
V_{IH}
V_{IL}
V_{OL}
70
75
80
85
90
95
β_F

Fig. 16(b)
T = 27°C

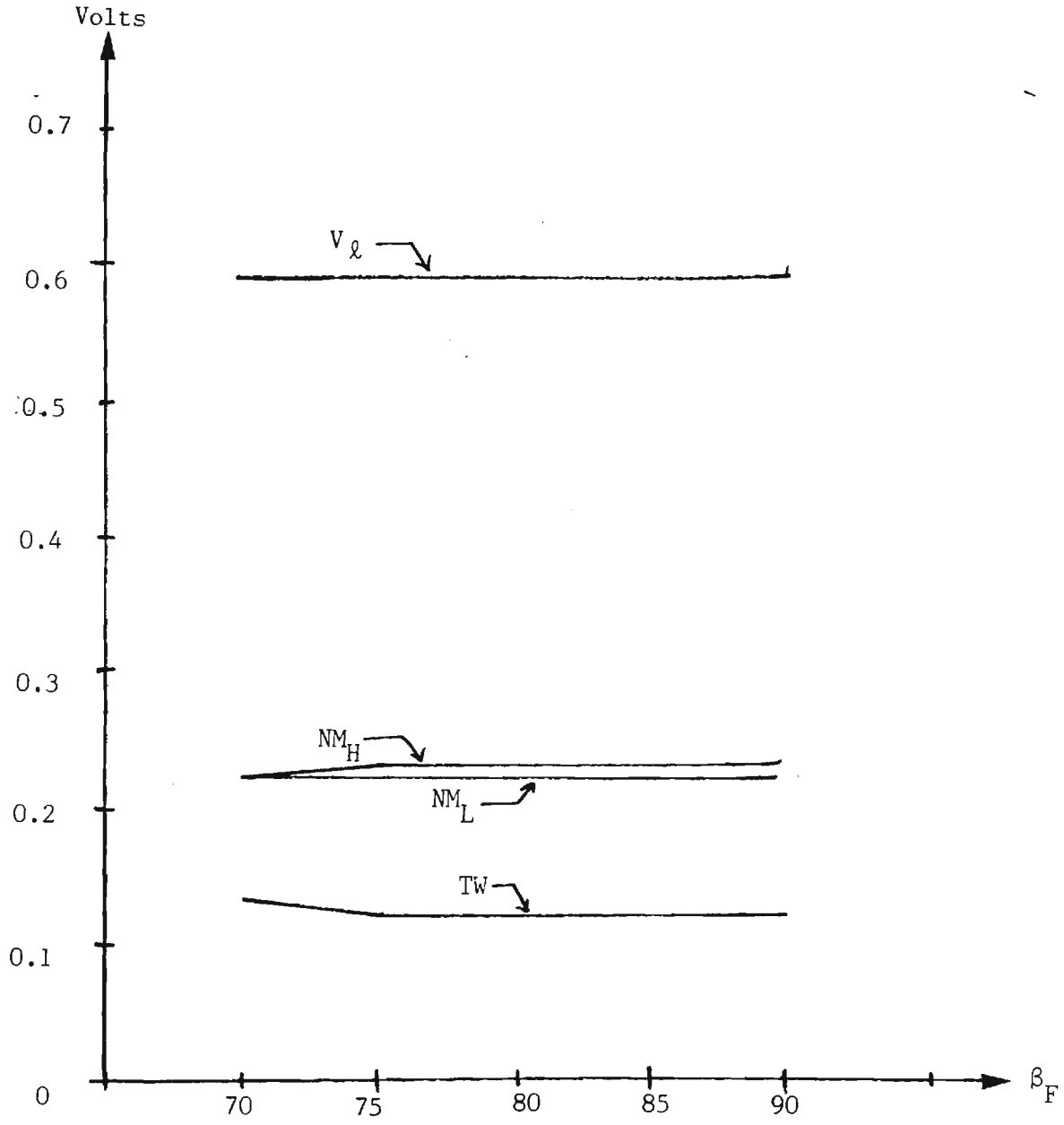


Fig. 16(b)-Continued
T = 27°C

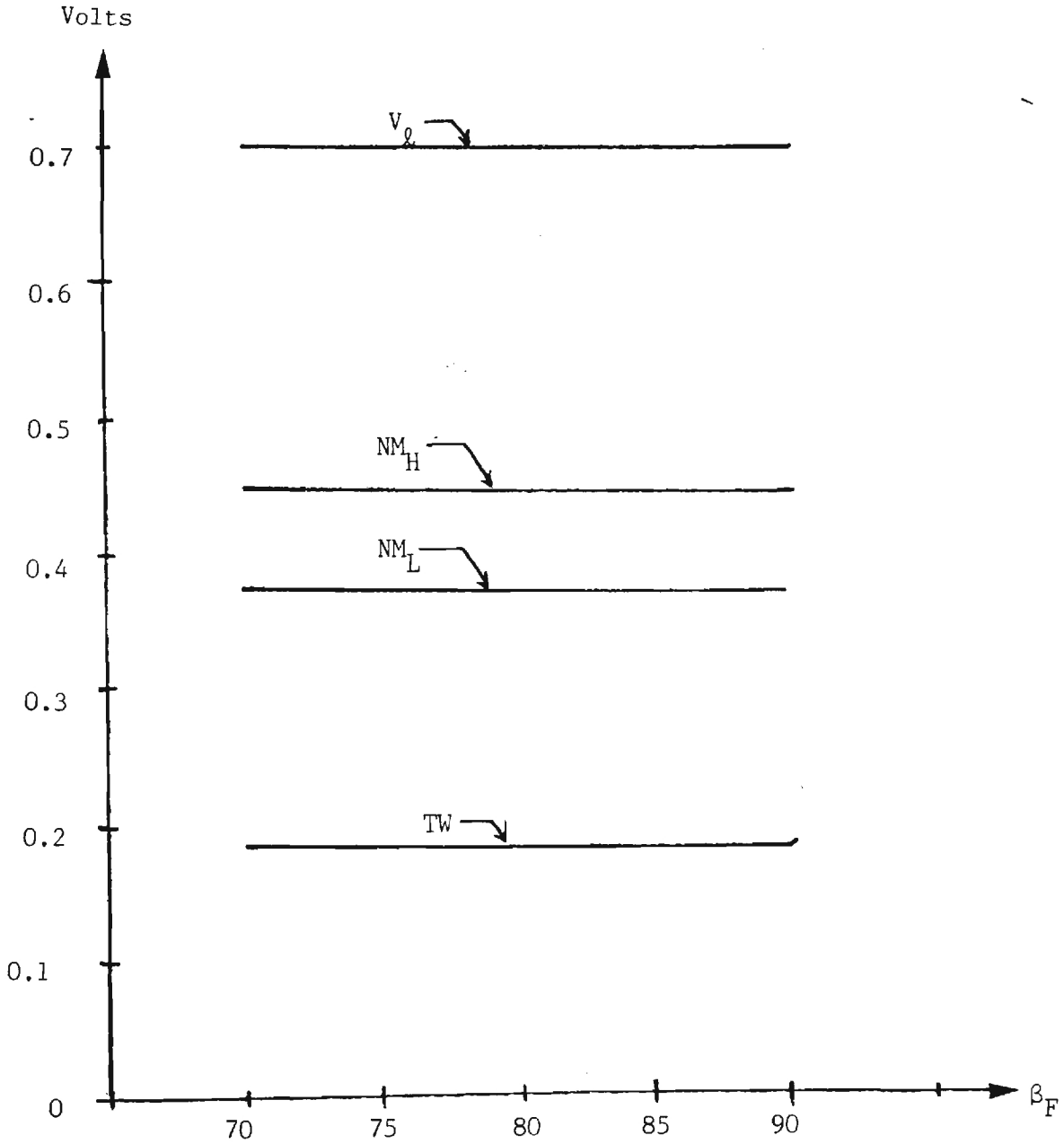


Fig. 16(c)
T = 85°C

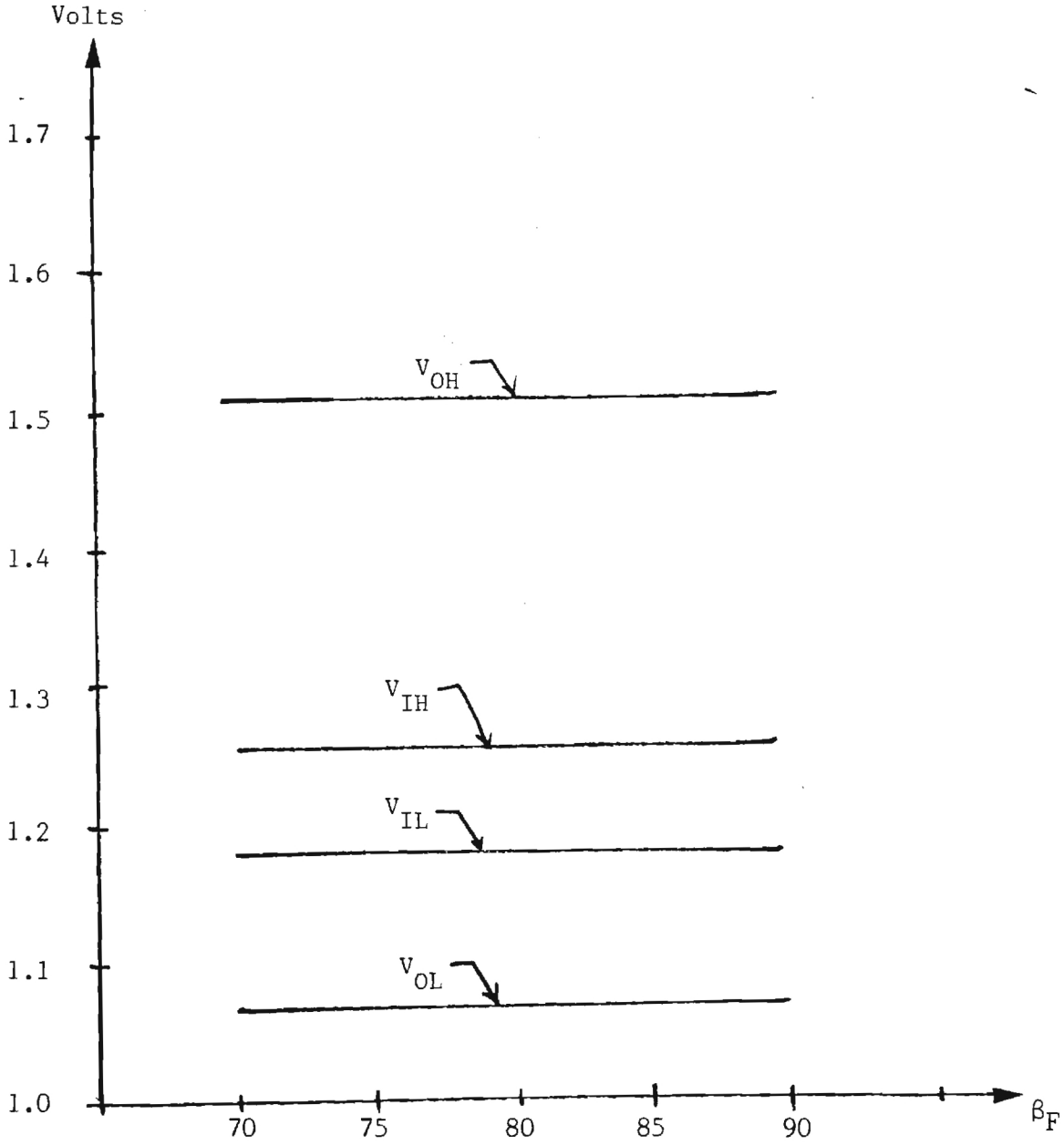


Fig. 16(c)-Continued
$t = 85^{o}C$

Figure 16

VTC Dependence Upon Current Gain β_F

V_{jE}= 0.7 [V], r_B= 150 [Ω], r_C= 100 [Ω], I_S= 2.93 [fA]
n_F=1.008 , I_{KF}=2 x 10^{-3}

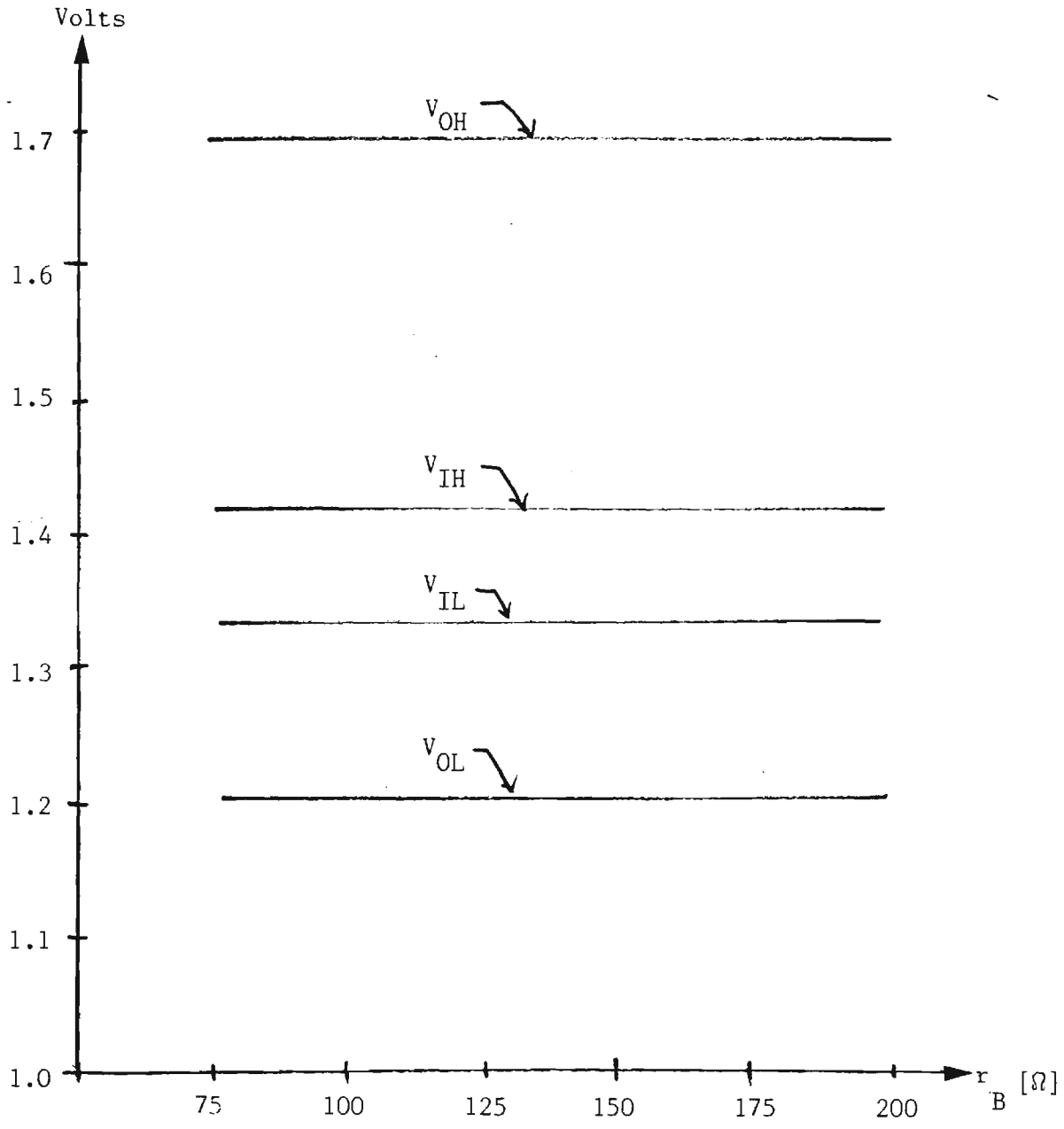

Volts
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
V_{OH}
V_{IH}
V_{IL}
V_{OL}
75
100
125
150
175
200
r_B [Ω]

Fig. 17(a)
T= 10°C

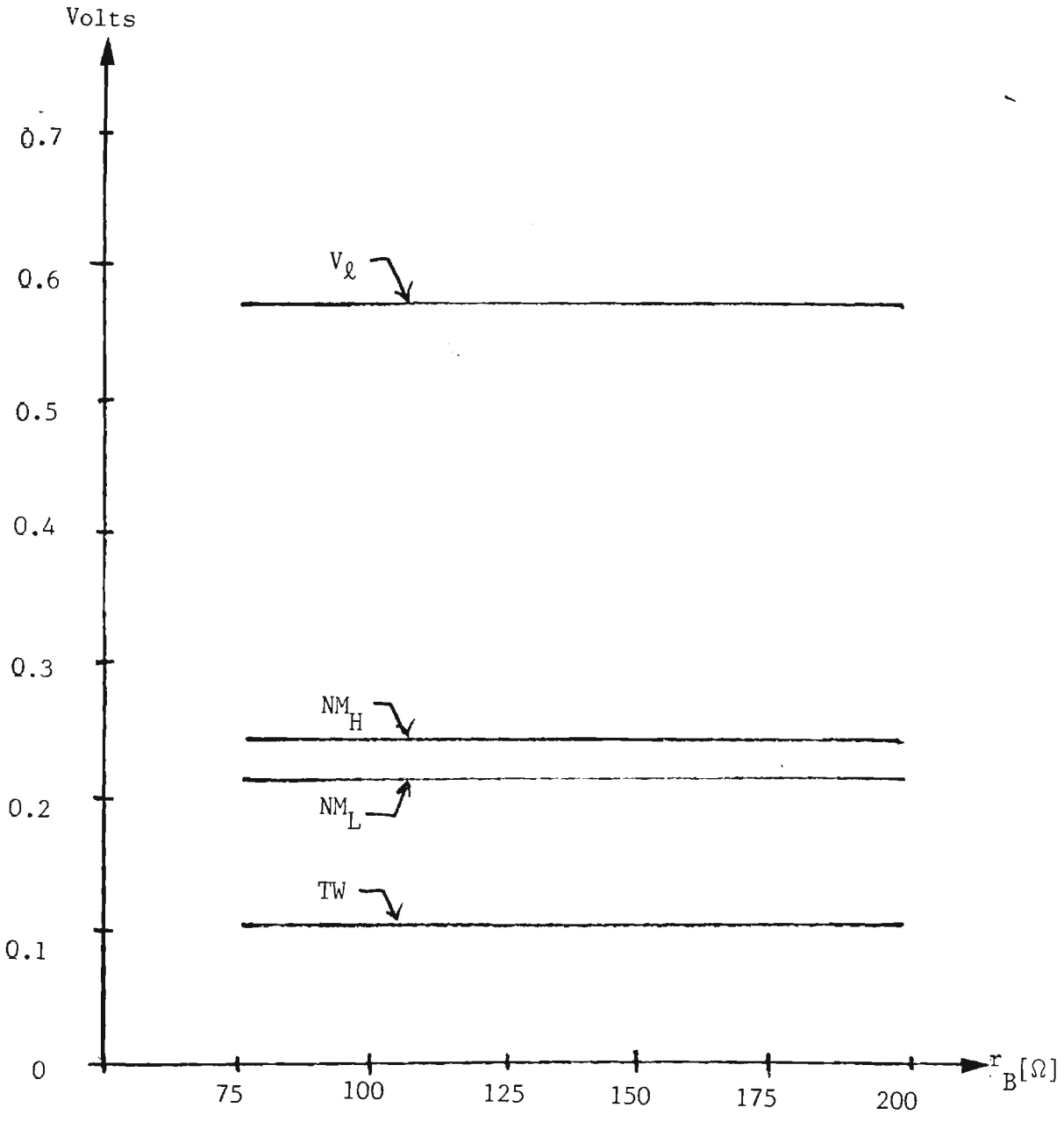


Fig. 17(a)-Continued
T = 10°C

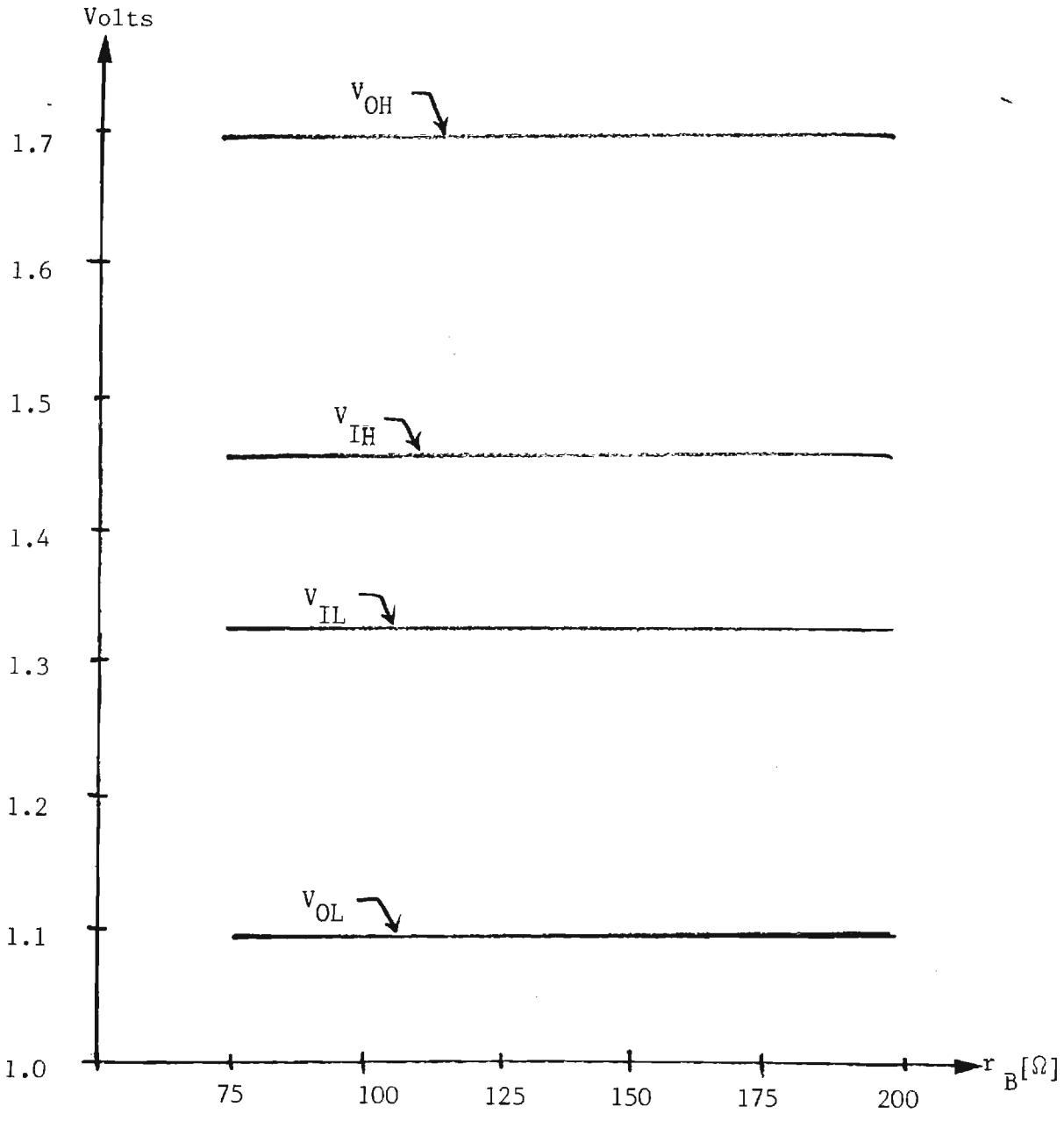

Volts
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
V_{OH}
V_{IH}
V_{IL}
V_{OL}
75
100
125
150
175
200
$r_B[\Omega]$

Fig. 17(b)
T =27°C

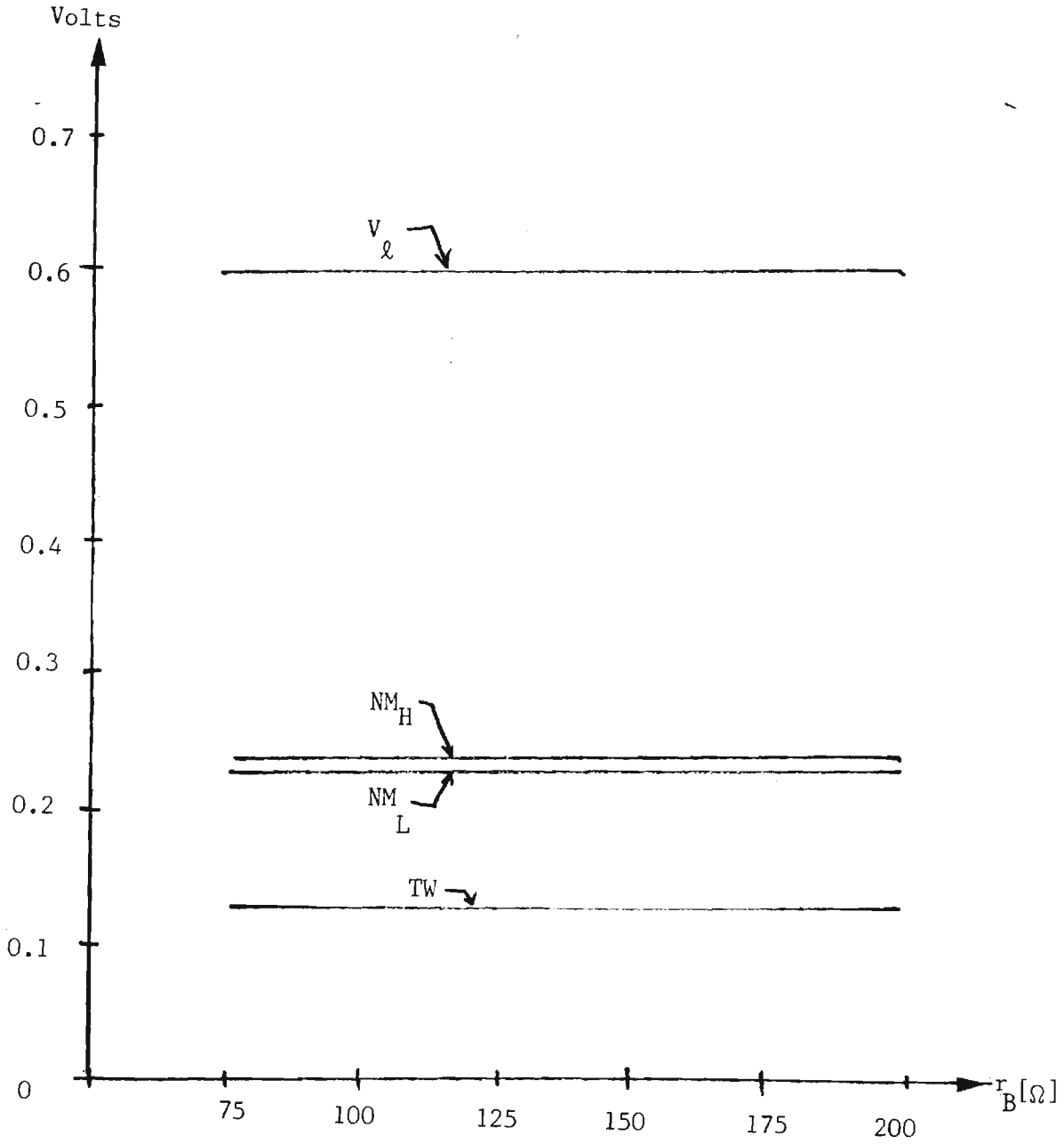


Fig. 17(b)-Continued
T = 27°C

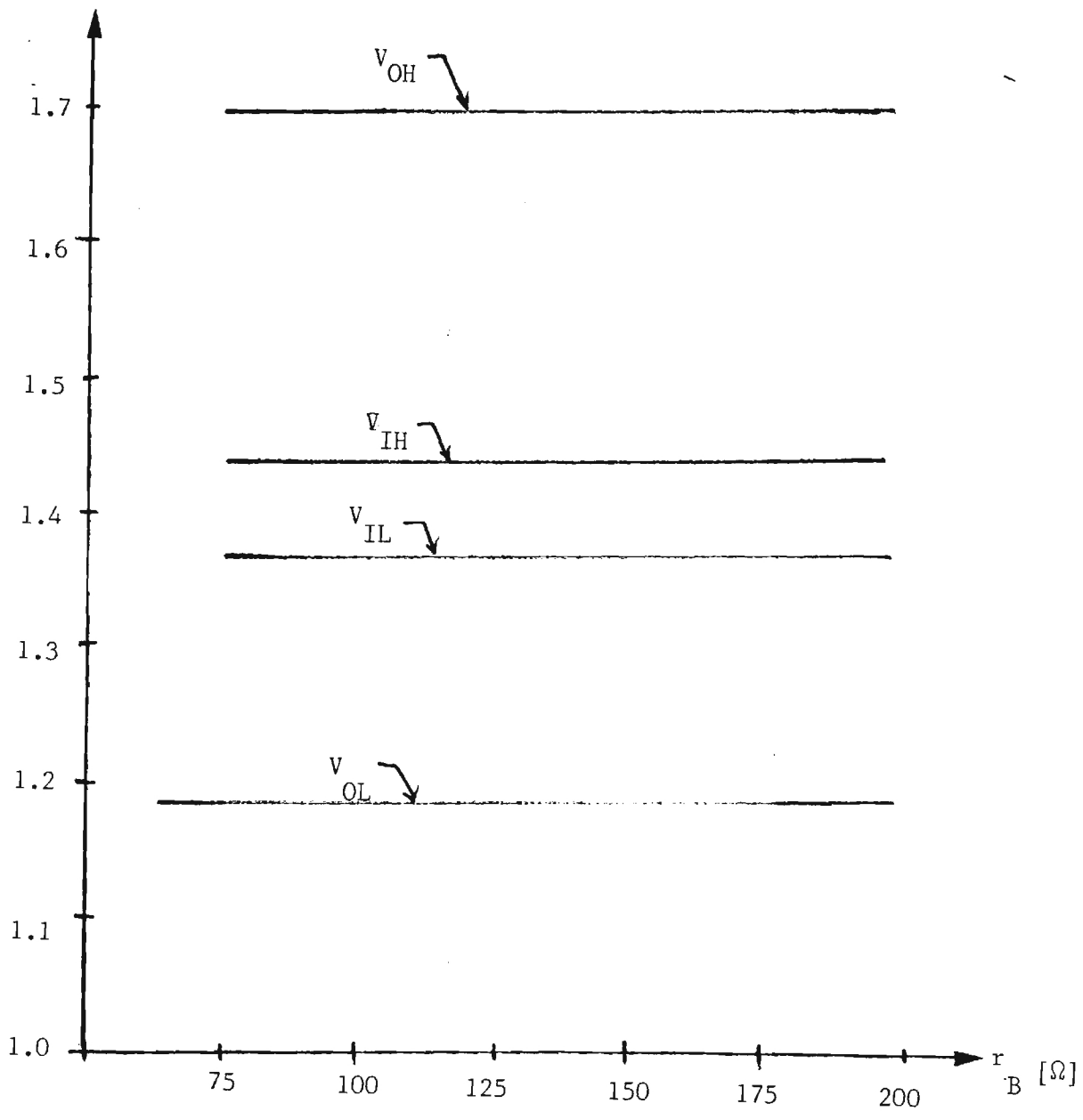


Fig. 17(c)
T = 85°C

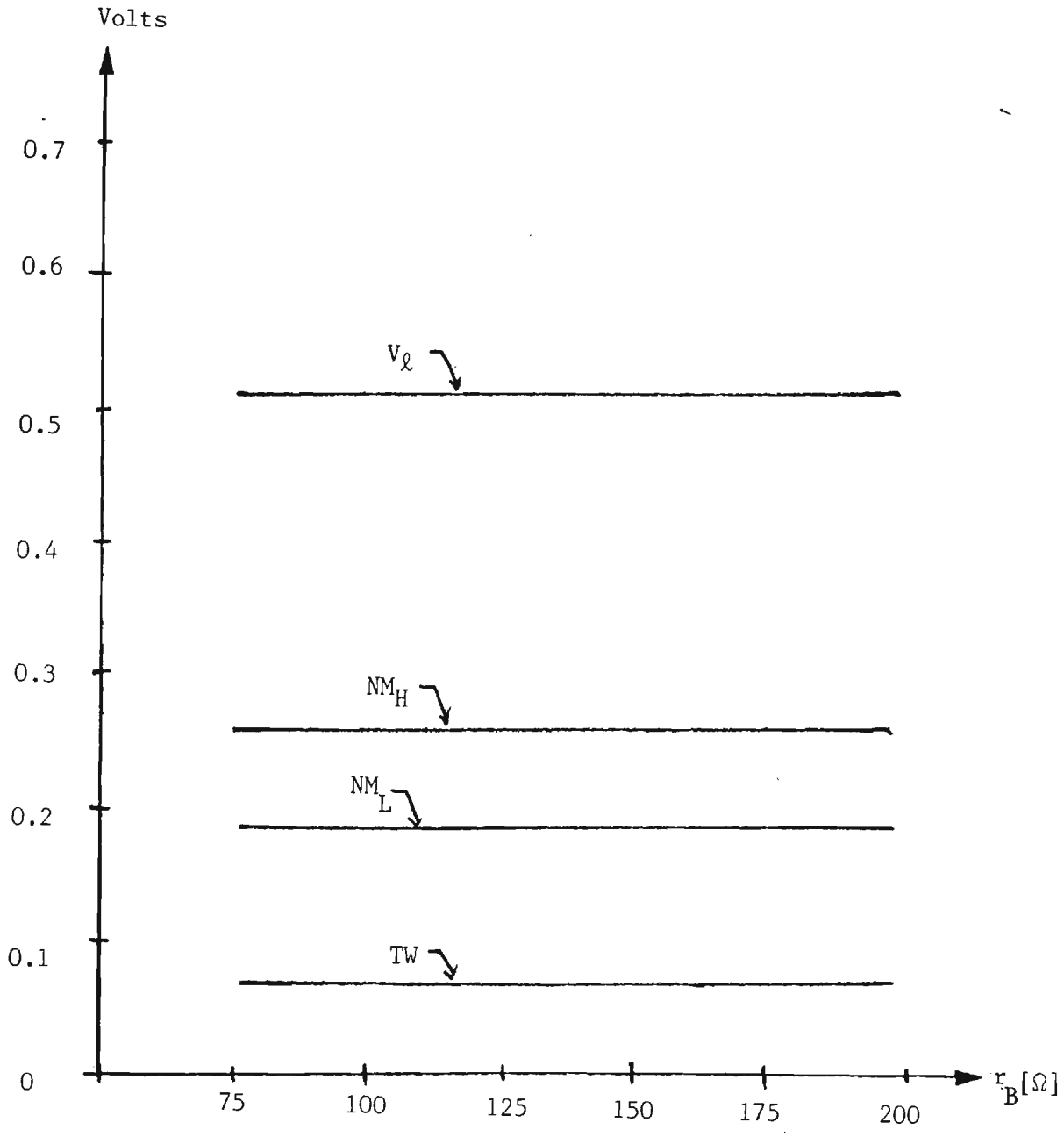


Fig. 17(c)-Continued
$T=85^{o}C$

Figure 17

VTC Dependence on r_B

V_{jE}= 0.7 [V], I_S= 2.93 [fA], r_c= 100[Ω], β_F= 80
η_F= 1.008, I_{KF} =2 x 10^{-3}

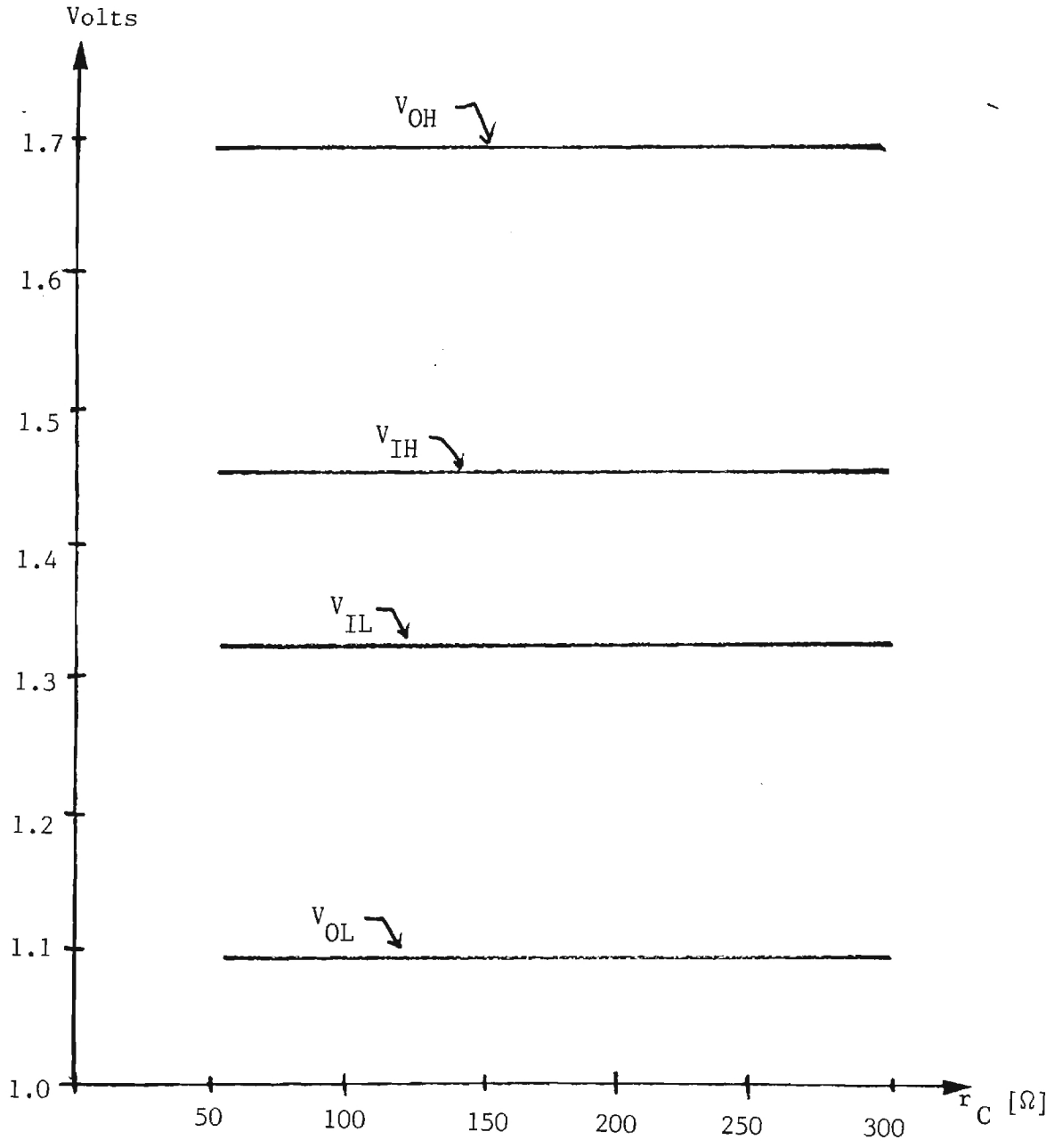

Volts
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
V_{OH}
V_{IH}
V_{IL}
V_{OL}
50
100
150
200
250
300
r_C [Ω]

Fig. 18

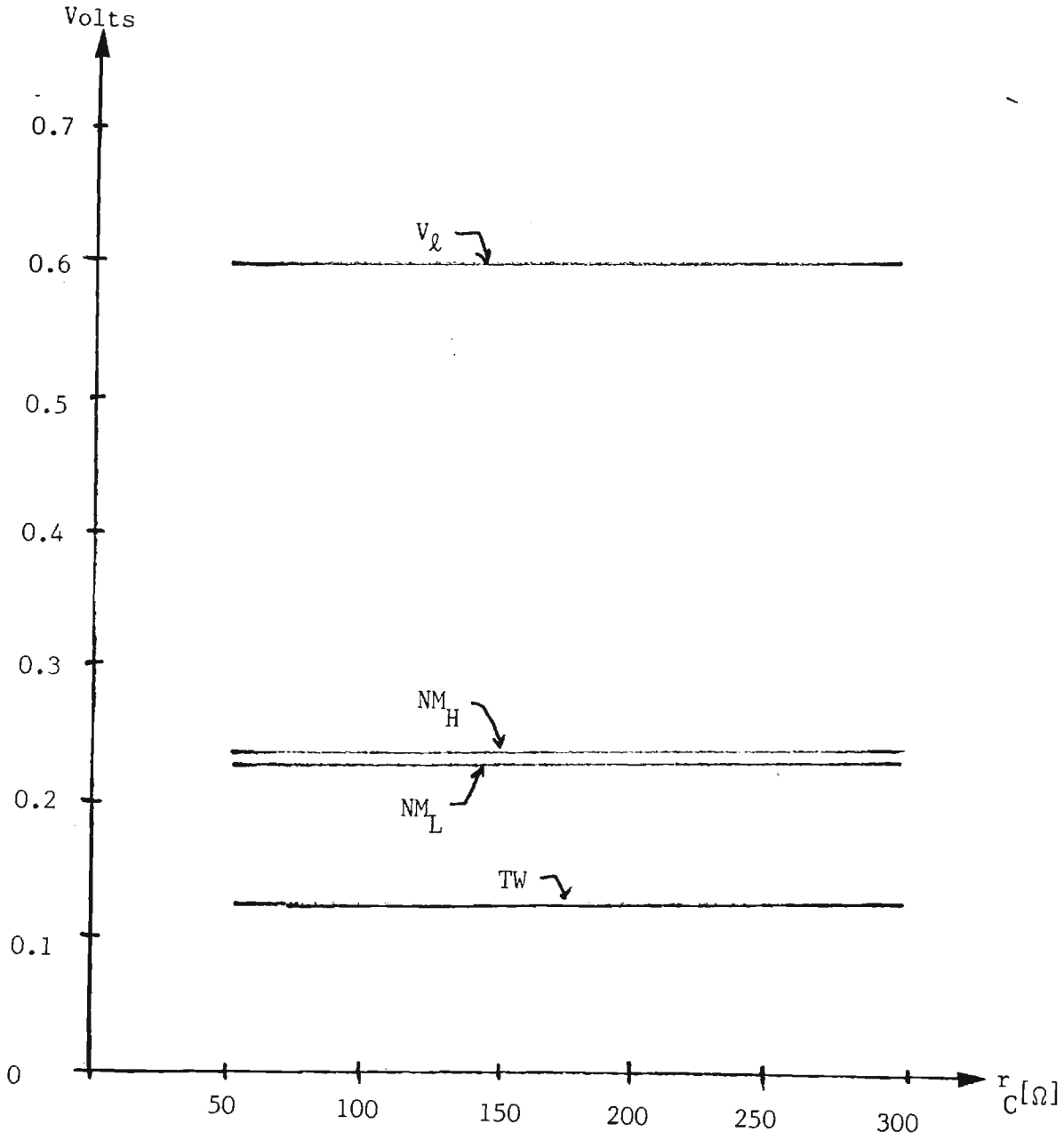


Figure 18

VTC Dependence on r_C

$T=27^oC$, $V_{jE}= 0.7$ [V], $r_B= 150$ [Ω], $I_S=2.93$ [fA],

$\beta_F=80$, $\eta_F=1.008$, $I_{KF} = 2 \times 10^{-3}$

Two parameters which were found to be important to the VTC analysis were I_{KF} and η_F. These appear in the level 2 SPICE model of a bipolar transistor and are important for describing forward-active operation. To understand these two parameters, note that the SPICE program computes transistor collector currents by means of the equation

$$I_C \simeq \frac{I_S}{Q_B} e^{V_{BE}/\eta_F V_T} \qquad (6\text{-}2)$$

when the device is biased into conduction. The approximate sign is used in the analytic expression to make note of the fact that some terms have been ignored for the current discussion. Although the SPICE parameter list terms η_F the Forward Current Emission Coefficient, it is immediately recognized as what is commonly called an "ideality factor" which accounts for the behavior of the base-emitter depletion region.

The quantity Q_B in eqn. (6-2) is not a charge, but rather is given by

$$Q_B = \frac{1}{2} Q_1 [1 + \sqrt{1 + 4Q_2}\,] \qquad (6\text{-}3)$$

where Q_1 is an Early Voltage factor

$$Q_1 = [1 - \frac{V_{BE}}{V_{AR}} - \frac{V_{BC}}{V_{AF}}]^{-1} \qquad (6\text{-}4)$$

and Q_2 accounts for beta roll-off by means of

$$Q_2 = \frac{I_S}{I_{KF}} \left(e^{V_{BE}/\eta_F V_T} - 1\right) + \frac{I_S}{I_{KR}} \left(e^{V_{BC}/\eta_R V_T} - 1\right) , \quad (6\text{-}5)$$

Assuming that the Early Voltages are infinite so that $Q_1 = 1$ is a good approximation, the collector current in forward-active bias is given roughly by the expression

$$I_C \simeq \frac{2I_S}{\left(1 + \sqrt{1 + 4 \frac{I_S}{I_{KF}} e^{V_{BE}/\eta_F V_T}}\right)} e^{V_{BE}/\eta_F V_T} , \quad (6\text{-}6)$$

This clearly demonstrates the sensitivity of the current flow with regards to these two parameters; note also that I_S will be important. By inspection, the VTC should be more sensitive to variations in η_F than those in I_{KF}.

The SPICE results for changes in I_{KF} are shown in Fig. 19, while η_F variations are demonstrated in Fig. 20. It should be noted that the plot of η_F ranges from 0.8 to 1.3, which represent approximate limits extrapolated for the current flow levels of $I_{EE} = 1.0$[mA].

The results of this section are summarized in Tables 2 - 4 for convenience in future reference. The basic conclusions are that I_S and η_F induce major effects, I_{KF} and β_F are responsible for small changes, while the remaining parameters are relatively unimportant. The value of I_S is most closely related to the magnitude of I_C, while η_F is responsible for the shape of the transistor transfer curve. Of course, temperature variations also affect the performance of the circuit.

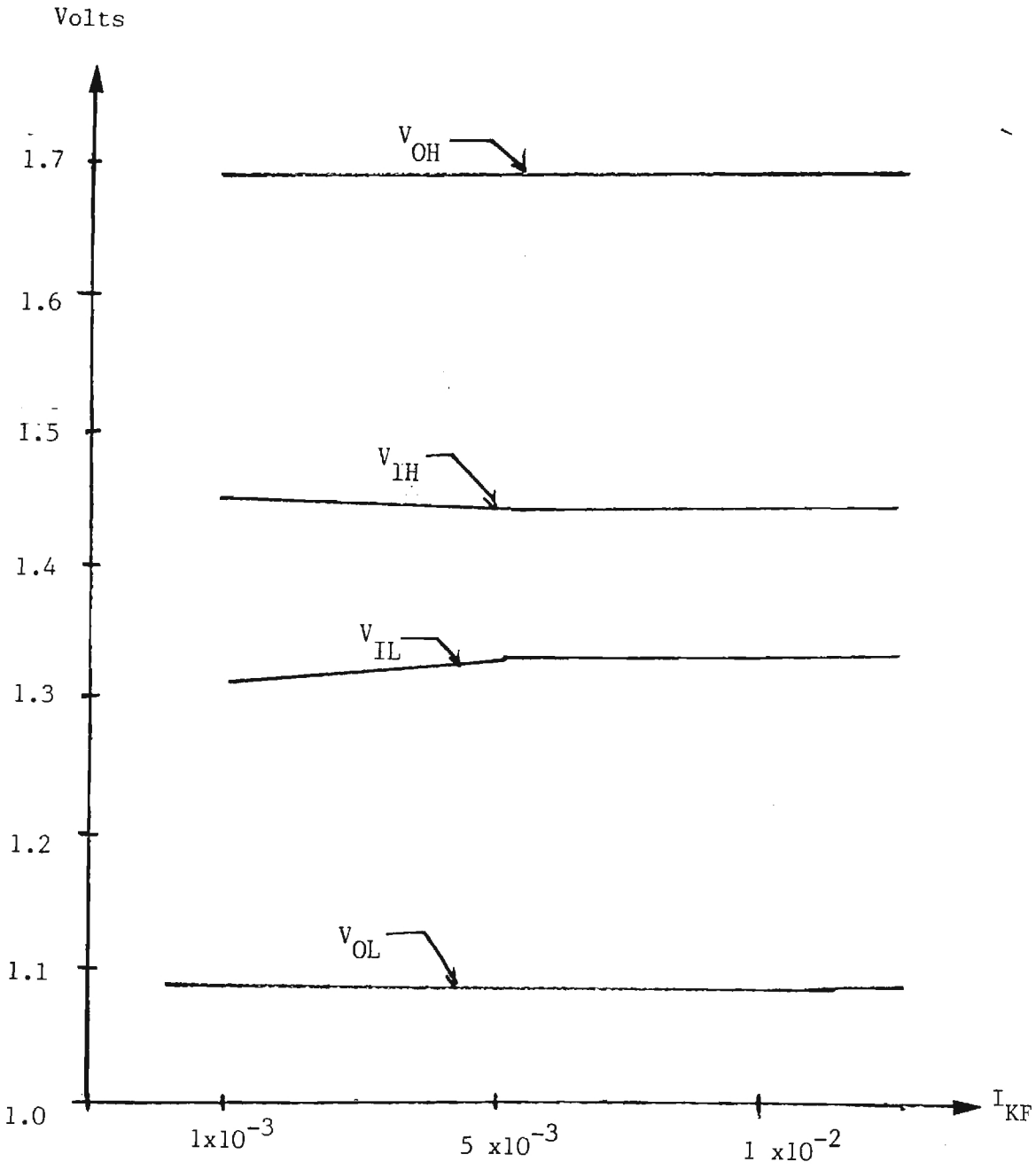

Volts
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
V_{OH}
V_{1H}
V_{IL}
V_{OL}
$1x10^{-3}$
$5\ x10^{-3}$
$1\ x10^{-2}$
I_{KF}

Fig. 19

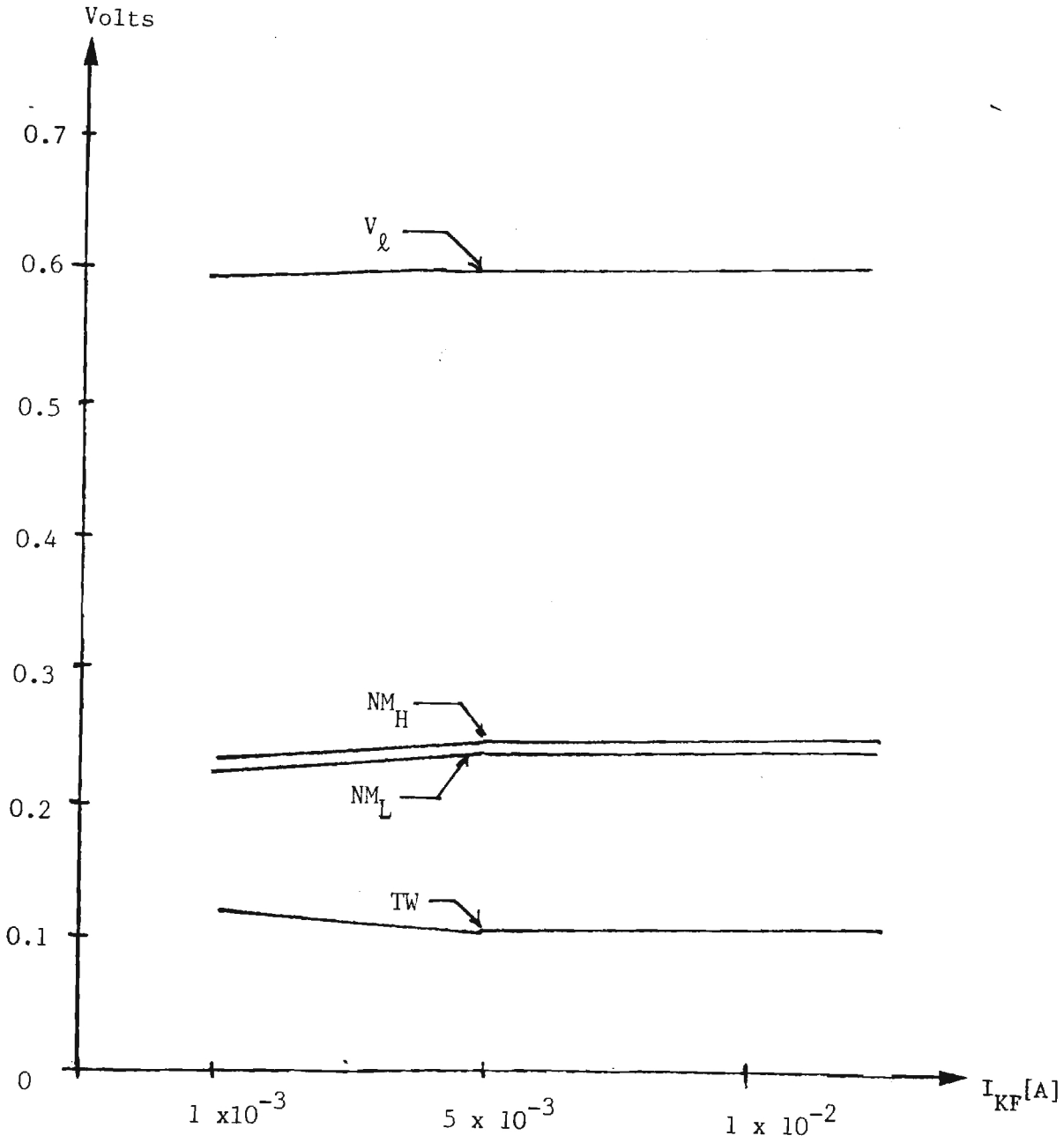


Figure 19

VTC Dependence on I_{KF}

T=27°C, V_{jE}= 0. 7[V], r_B= 150 [Ω], r_C= 100 [Ω],
I_S= 2.93 [fA], β_F= 80, η_F= 1.008

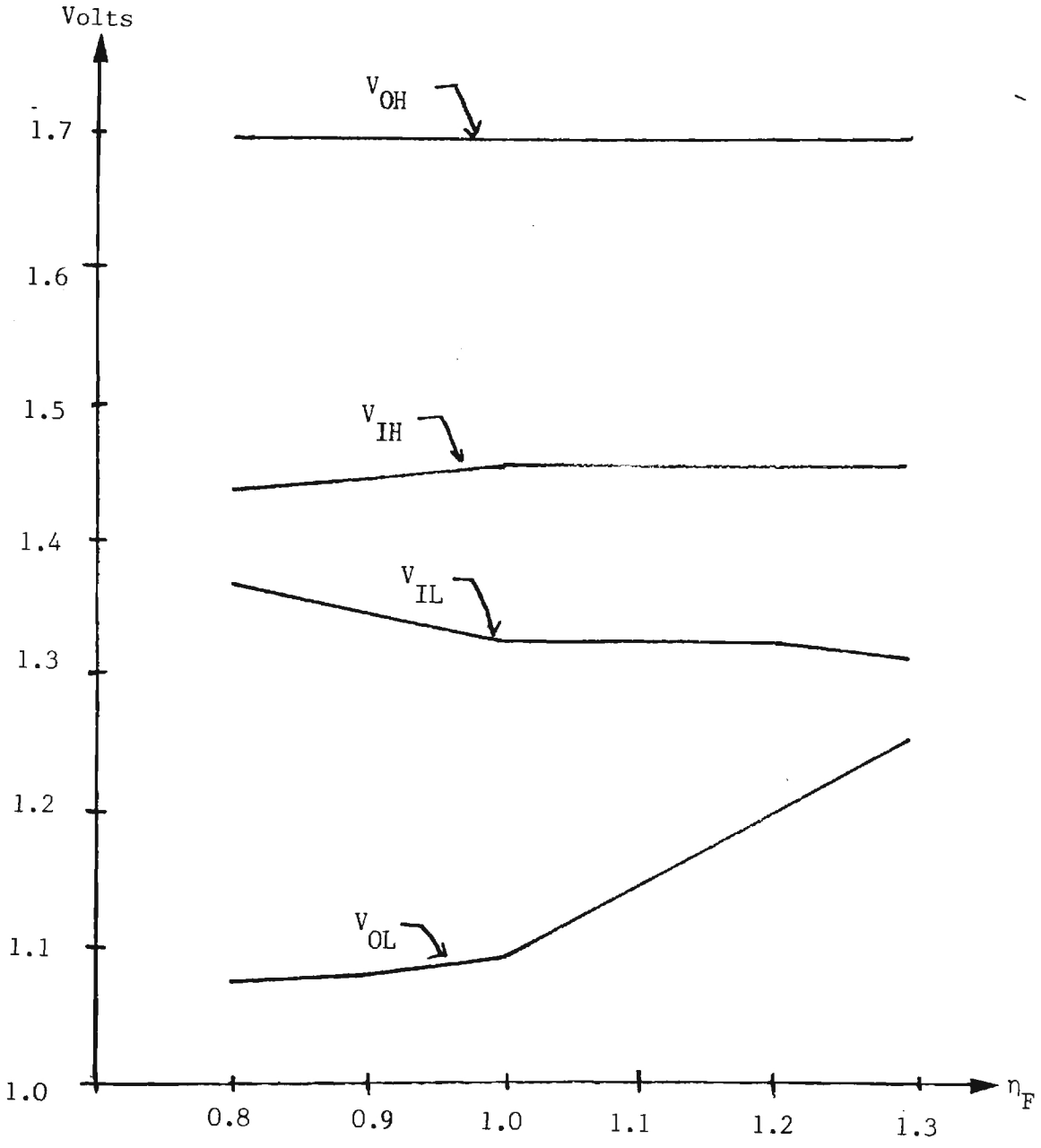


Fig. 20

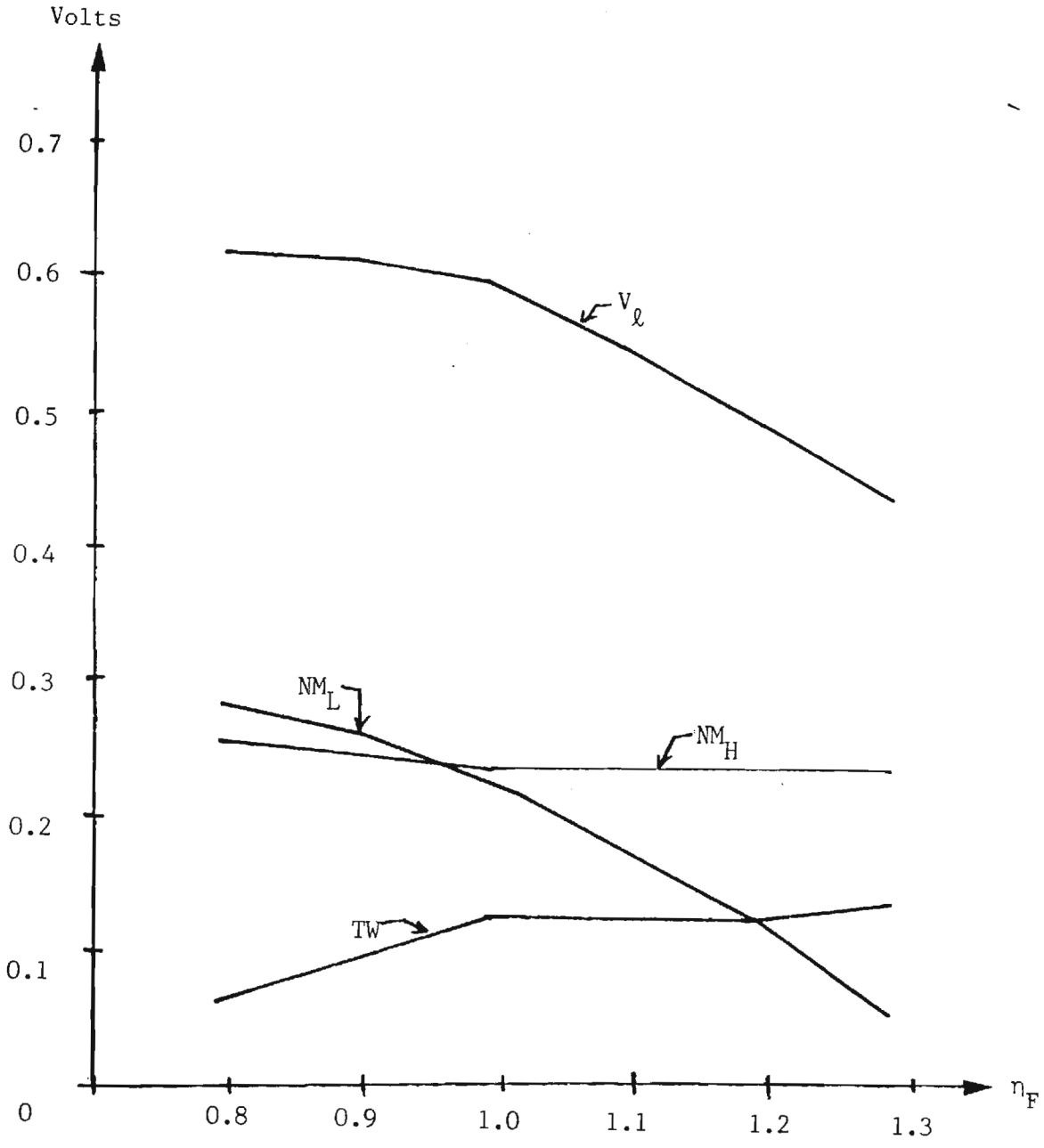


Figure 20

VTC Dependence on η_F

$T=27^oC$, $V_{jE}= 0.7$ [V], $r_B= 150$ [Ω], $r_C= 100$ [Ω],
$I_S=2.93$ [fA], $\beta_F = 80$, $I_{KF} = 2 \times 10^{-3}$ [mA]

V_{je} = .70 [V] r_B = 150 [Ω] r_C = 100 [Ω] I_S = 2.93 [fA]

β_F	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
70	1.70	1.123	1.45	1.34	250	217	110	577
75	1.70	1.122	1.45	1.34	250	218	110	578
80	1.70	1.122	1.45	1.34	250	218	110	578
85	1.70	1.121	1.45	1.34	250	219	110	579
90	1.70	1.121	1.45	1.34	250	219	110	579

β_F = 80 r_B = 150 [Ω] r_C = 100 [Ω] I_S = 2.93 [fA]

V_{je}	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
.68	1.70	1.122	1.45	1.34	250	218	110	578
.70	1.70	1.122	1.45	1.34	250	218	110	578
.72	1.70	1.122	1.45	1.34	250	218	110	578
.74	1.70	1.122	1.45	1.34	250	218	110	578
.76	1.70	1.122	1.45	1.34	250	218	110	578
.78	1.70	1.122	1.45	1.34	250	218	110	578
.80	1.70	1.122	1.45	1.34	250	218	110	578

Table 2
T = 10° C

V_{je} = .7 [V] r_B = 150 [Ω] r_C = 100 [Ω] β_F = 80

I_S [fA]	V_{OH} [V]	V_{OL} [V]	V_{OH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
.1	1.70	1.188	1.45	1.34	250	152	110	512
.5	1.70	1.156	1.45	1.34	250	184	110	544
.1	1.70	1.143	1.45	1.34	250	197	110	557
2.93	1.70	1.121	1.45	1.34	250	219	110	579
.5	1.70	1.111	1.45	1.34	250	229	110	589
10	1.70	1.097	1.45	1.34	250	243	110	603
50	1.70	1.066	1.45	1.34	250	274	110	634

V_{je} = .7 [V] I_S = 2.93 [fA] r_C = 100 [Ω] β_F = 80

r_B	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
75	1.70	1.121	1.45	1.34	250	219	110	579
100	1.70	1.121	1.45	1.34	250	219	110	579
125	1.70	1.121	1.45	1.34	250	219	110	579
150	1.70	1.121	1.45	1.34	250	219	110	579
175	1.70	1.121	1.45	1.34	250	219	110	579
200	1.70	1.121	1.45	1.34	250	219	110	579
	1.70	1.121	1.45	1.34	250	219	110	579

Table 2

Summary of Basic ECL Variations
for T = 10°

V_{je} = .70 [V] r_B = 150 [Ω] r_C = 100 [Ω] I_S = 2.93 [fA] NF = 1.008 1KF = 2x10

F	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
70	1.70	1.10	1.47	1.33	230	230	140	600
75	1.70	1.10	1.46	1.33	240	230	130	600
80	1.70	1.098	1.46	1.33	240	232	130	602
85	1.70	1.098	1.46	1.33	240	232	130	602
90	1.70	1.097	1.46	1.33	240	233	130	603

β_F = 80 r_B = 150 [Ω] r_C = 100 [Ω] I_S = 2.93 [fA] NF = 1.008 1KF = $2x10^{-3}$

V_{je}	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
.68	1.70	1.098	1.46	1.33	240	232	130	602
.70	1.70	1.098	1.46	1.33	240	232	130	602
.72	1.70	1.098	1.46	1.33	240	232	130	602
.74	1.70	1.098	1.46	1.33	240	232	130	602
.76	1.70	1.098	1.46	1.33	240	232	130	602
.78	1.70	1.098	1.46	1.33	240	232	130	602
.80	1.70	1.098	1.46	1.33	240	232	130	602

Table 3

T= 27°

V_{je} = .7 [V] r_B = 150 [Ω] r_C = 100 [Ω] β_F = 80 NF = 1.008 1KF = 2×10^{-3}

I_S [fA]	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
.1	1.70	1.169	1.45	1.34	250	171	110	531
.5	1.70	1.135	1.45	1.33	250	195	120	565
.1	1.70	1.121	1.45	1.33	250	209	120	579
2.93	1.70	1.098	1.46	1.33	240	232	130	602
.5	1.70	1.091	1.46	1.33	240	239	130	609
10	1.70	1.092	1.47	1.34	230	248	130	608
50	1.70	1.092	1.45	1.35	250	258	100	608

V_{je} = .7 [V] I_S = 2.93 [fA] r_C = 100 [Ω] β_F = 80

r_B	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
75	1.70	1.098	1.46	1.33	240	232	130	602
100	1.70	1.098	1.46	1.33	240	232	130	602
125	1.70	1.098	1.46	1.33	240	232	130	602
150	1.70	1.098	1.46	1.33	240	232	130	602
175	1.70	1.099	1.46	1.33	240	231	130	601
200	1.70	1.099	1.46	1.33	240	231	130	601
225	1.70	1.099	1.46	1.33	240	231	130	601

Table 3

T = 10°

V_{je} = .70 [V] r_B = 150 [Ω] I_S = 2.93 [fA] β_F = 80 NF = 1.008 1KF = $2x10^{-3}$

r_C	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
50	1.70	1.098	1.46	1.33	240	232	130	60
75	1.70	1.098	1.46	1.33	240	232	130	602
100	1.70	1.098	1.46	1.33	240	232	130	602
150	1.70	1.098	1.46	1.33	240	232	130	602
200	1.70	1.098	1.46	1.33	240	232	130	602
250	1.70	1.098	1.46	1.33	240	232	130	602
300	1.70	1.098	1.46	1.33	240	232	130	602

V_{je} = .70 [V] r_B = 150 [Ω] r_C = 100 [Ω] I_S = 2.93 [fA] β_F = 80 1KF = $2x10^{-3}$

NF	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
.8	1.70	1.080	1.44	1.37	260	290	70	620
.9	1.70	1.085	1.45	1.35	250	265	100	615
1.008	1.70	1.148	1.46	1.33	240	182	130	602
1.1	1.70	1.148	1.46	1.33	240	182	130	552
1.2	1.70	1.202	1.46	1.33	240	128	130	498
1.3	1.70	1.258	1.46	1.32	240	62	140	442

Table 3

T=10°

V_{je} = .70 [V] r_B = 150 [Ω] r_C = 100 [Ω] I_S = 2.93 [fA] β_F = 80 NF = 1.008

IKF [A]	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
2×10^{-3}	1.70	1.098	1.46	1.33	240	232	130	602
5×10^{-3}	1.70	1.095	1.45	1.34	250	245	110	605
1×10^{-2}	1.70	1.093	1.45	1.34	250	247	110	607
1.5×10^{-2}	1.70	1.093	1.45	1.34	250	247	110	607
2×10^{-2}	1.70	1.092	1.45	1.34	250	248	110	608

Table 3

Summary of Basic ECL Variations
for T = 10°

V_{je} = .70 [V] r_B = 150 [Ω] r_C = 100 [Ω] I_S = 2.93 [fA]

β_F	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
70	1.70	1.187	1.44	1.37	260	183	70	513
75	1.70	1.187	1.44	1.37	260	183	70	513
80	1.70	1.187	1.44	1.37	260	183	70	513
85	1.70	1.187	1.44	1.37	260	183	70	513
90	1.70	1.187	1.44	1.37	260	183	70	513

β_F = 80 r_B = 150 [Ω] r_C = 100 [Ω] I_S = 2.93 [fA]

V_{je}	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
.68	1.70	1.187	1.44	1.37	260	183	70	513
.70	1.70	1.187	1.44	1.37	260	183	70	513
.72	1.70	1.187	1.44	1.37	260	183	70	513
.74	1.70	1.187	1.44	1.37	260	183	70	513
.76	1.70	1.187	1.44	1.37	260	183	70	513
.78	1.70	1.187	1.44	1.37	260	183	70	513
.80	1.70	1.187	1.44	1.37	260	183	70	513

Table 4
T=10°

V_{je} = .70 [V] r_B = 150 [Ω] r_C = 100 [Ω] β_F = 80

I_S [fA]	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
.1	1.70	1.186	1.46	1.36	240	174	100	514
.5	1.70	1.186	1.45	1.36	250	174	90	514
.1	1.70	1.186	1.44	1.37	260	184	70	514
2.93	1.70							
.5	1.70	1.187	1.44	1.38	260	193	60	513
10	1.70	1.187	1.43	1.38	270	193	50	513
50	1.70	1.189	1.43	1.38	270	191	50	511

V_{je} = .7 [V] I_S = 2.93 [fA] r_C = 100 [Ω] β_F = 80

r_B	V_{OH} [V]	V_{OL} [V]	V_{IH} [V]	V_{IL} [V]	NM_H [mV]	NM_L [mV]	TW [mV]	V_L [mV]
75	1.70	1.187	1.44	1.37	260	183	70	513
100	1.70	1.187	1.44	1.37	260	183	70	513
125	1.70	1.187	1.44	1.37	260	183	70	513
150	1.70	1.187	1.44	1.37	260	183	70	513
175	1.70	1.187	1.44	1.37	260	183	70	513
200	1.70	1.187	1.44	1.37	260	183	70	513
225	1.70	1.187	1.44	1.37	260	183	70	513

Table 4

Summary of Basic ECL Variations
for t=10°

7. Analysis of SPICE Results

It was demonstrated in the previous section that the critical VTC values show the greatest change when I_S and η_F are varied. It is possible to study this dependence in more detail by applying straightforward device models. The simplest approach is based on the approximate transistor equation

$$I_C \simeq I_S \, e^{V_{BE}/\eta_F V_T} \tag{7-1}$$

which includes the two parameters of interest. Taking differentials of both sides gives

$$dI_C \simeq \frac{\partial I_C}{\partial I_S} \, dI_S + \frac{\partial I_C}{\partial \eta_F} \, d\eta_F \tag{7-2}$$

or, in terms of finite changes,

$$\Delta I_C \simeq e^{V_{BE}/\eta_F V_T} \, (\Delta I_S) - I_S e^{V_{BE}/\eta_F V_T} \, \frac{V_{BE}}{\eta_F^2 V_T} \, (\Delta \eta_F) \quad . \tag{7-3}$$

This may be rearranged to read

$$\frac{\Delta I_C}{I_C} \simeq \frac{\Delta I_S}{I_S} - \frac{V_{BE}}{\eta_F V_T} \, \frac{\Delta \eta_F}{\eta_F} \tag{7-4}$$

which clearly illustrates the dependence of I_C on the two varying parameters. This equation shows that ΔI_S and $\Delta \eta_F$ oppose each other,

The collector current variations are thus expressed as

$$\frac{\Delta I_C}{I_C} \simeq - \frac{\Delta N_G}{N_G} - \frac{V_{BE}}{\eta_F V_T} \frac{\Delta \eta_F}{\eta_F} \qquad (7\text{-}9)$$

to this order of approximation. It is important to note that the Gummel number N_G depends upon the acceptor doping profile $N_a(x)$ in the base, making it sensitive to processing variations. The quasi-neutral base width W is affected by the processing, but is also dependent upon the operating bias. These will be discussed in detail below.

The full variational dependence for this simplified model is found by writing $I_S = I_S(A_E, T, N_G)$ so that

$$dI_S = \frac{\partial I_S}{\partial A_E} dA_E + \frac{\partial I_S}{\partial T} dT + \frac{\partial I_S}{\partial N_G} dN_G \quad , \qquad (7\text{-}10)$$

The emitter area A_E is an alignment-error variable, while the temperature dependence is an environmental factor set by the operating bias and power dissipation. Using eqn. (7-6) gives directly that

$$\Delta I_S \simeq \frac{q\tilde{D}_n n_i^2}{N_G} (\Delta A_E) + \frac{qA_E\tilde{D}_n}{N_G} 2n_i(T) \frac{dn_i}{dT} (\Delta T)$$

$$- \frac{qA_E\tilde{D}_n n_i^2}{N_G} (\Delta N_G) \qquad (7\text{-}11)$$

where the intrinsic concentration is a temperature-dependent function

in the form

$$n_i^2(T) = K\,T^3\; e^{-E_g(T)/kT} \qquad (7\text{-}12)$$

with K=constant. Substituting the complete dependence of eqn. (7-11) into eqn. (7-4) then yields

$$\frac{\Delta I_C}{I_C} \simeq \frac{\Delta A_E}{A_E} + \frac{2}{n_i}\frac{dn_i}{dT}(\Delta T) - \frac{\Delta N_G}{N_G} - \frac{V_{BE}}{\eta_F V_T}\frac{\Delta \eta_F}{\eta_F}. \qquad (7\text{-}13)$$

This may be used directly to estimate the variations in the collector current. As a point of clarification, note that the "absolute" quantities such as I_C, A_E, N_G, etc., are the nominal values which would be used to design the circuit. The variations (ΔI_C, ΔA_E, etc.) represent the deviation from the nominal values.

The full significance of eqn. (7-13) is not apparent until each term is studied in more detail. However, all but the second term can be directly correlated with normal batch-to-batch processing variations. This comment may be understood by referring to the simplistic Gaussian distribution shown in Fig. 21 for the probability density $p(\xi)$ where

$$p(\xi) = \frac{1}{\sqrt{2\pi}\;\sigma}\; e^{-(\xi-m)^2/2\sigma^2} \qquad (7\text{-}14)$$

represents the distribution of a processing parameter. σ is the standard deviation of the distribution, while m is the mean or average value of the variable . The significance of this function is that $p(\xi)d\xi$

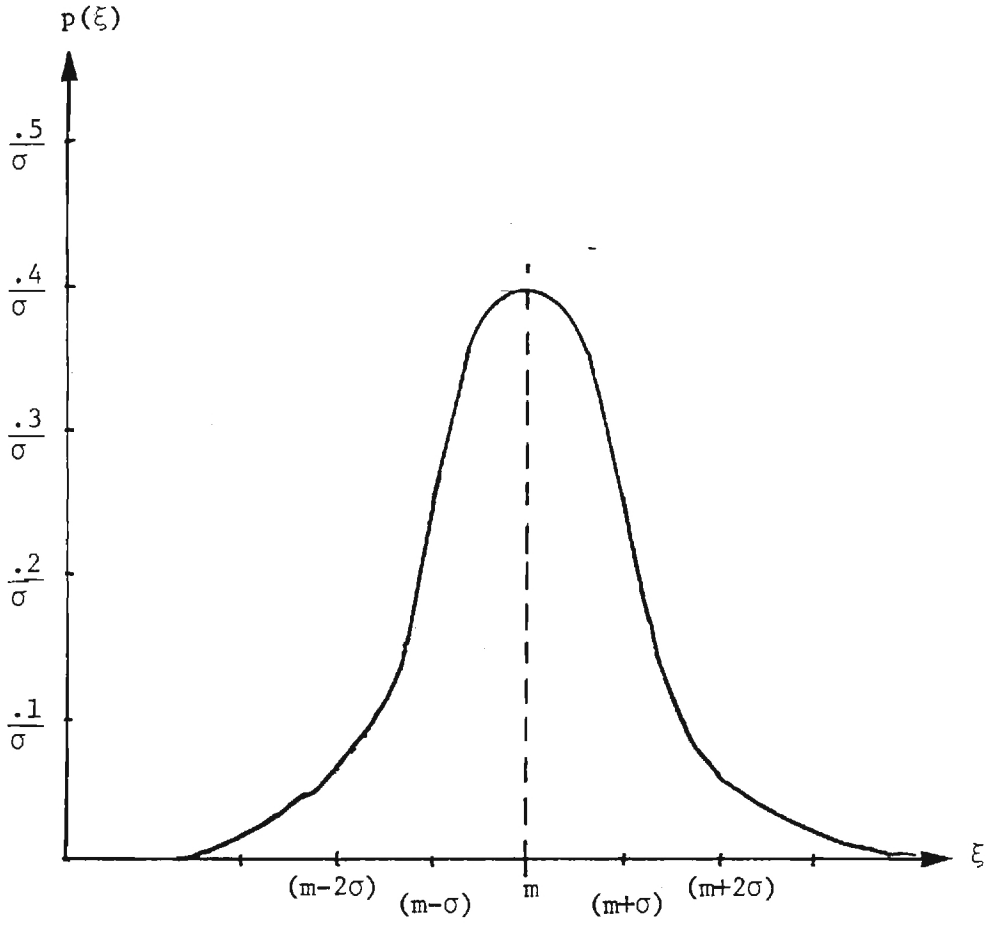


Figure 21

Gaussian Distribution

represents the probability of the parameter having a value between ξ and $(\xi+d\xi)$. With regards to integrated circuit process variations, m is usually associated with the nominal design value of a parameter, while the "3σ" spread gives the magnitude of the worst-case variation expected in batch-to-batch processing. The discussion below demonstrates the basic relations which exist between the processing and the expected circuit performance.

7.1 Gummel Number Variations

The Gummel number as defined by eqn. (7-7) is a complicated parameter as it incorporates two crucial bipolar transistor values, $N_a(x)$ and W. The variation ΔN_G may be estimated in a simple manner by assuming

$$N_a(x) = N_a'(x) + \delta N_a(x)$$
$$W = W_o + \delta W \qquad (7.1\text{-}1)$$

provide the variations in the doping and base width. Using these allows one to write

$$\Delta N_G \simeq \int_0^{W_o+\delta W} \delta N_a(x)dx + \int_{W_o}^{\delta W} N_a(x)\, dx \qquad (7.1\text{-}2)$$

as a first-order approximation to Gummel number variations. It is obvious that this simplistic treatment masks the true significance of ΔN_G; it is, however, a reasonable guess. Note that $\delta N_a(x)$ and

δW may be negative numbers. This allows for actual values of N_G to be greater than or less than the mean as needed in the distribution curve.

In order to analyze the significance of Gummel number variations, some analytic doping densities will be assumed for the typical bipolar transistor profile shown in Fig. 22; note that the origin has been shifted from that used earlier in Fig. 5. The n-type epitaxial layer is assumed to have a constant doping level N_{dC}. The base acceptor doping will be taken in Gaussian form

$$N_A(x) = N_{sA}\, e^{-x^2/d^2} \qquad (7.1\text{-}3)$$

where N_{sA} is the surface concentration while d is the characteristic length associated with the profile. This type of approximation would apply to a diffused base, but might also be used as a low order estimated for an annealled ion implanted p-type layer. The emitter n^+ doping will be assumed to be described by

$$N_{dE}(x) = N_{do}\, e^{-(x-R_p)^2/2(\Delta R_p)^2} \qquad (7.1\text{-}4)$$

corresponding to an ion implanted emitter. R_p is the projected range of the implant, ΔR_p is the straggle, and N_{do} is the peak doping level at R_p. Although a disjoint Gaussian is a better approximation for the emitter implant, it is a bit too messy in the analysis.

In computing the Gummel number, it is noted that the net acceptor

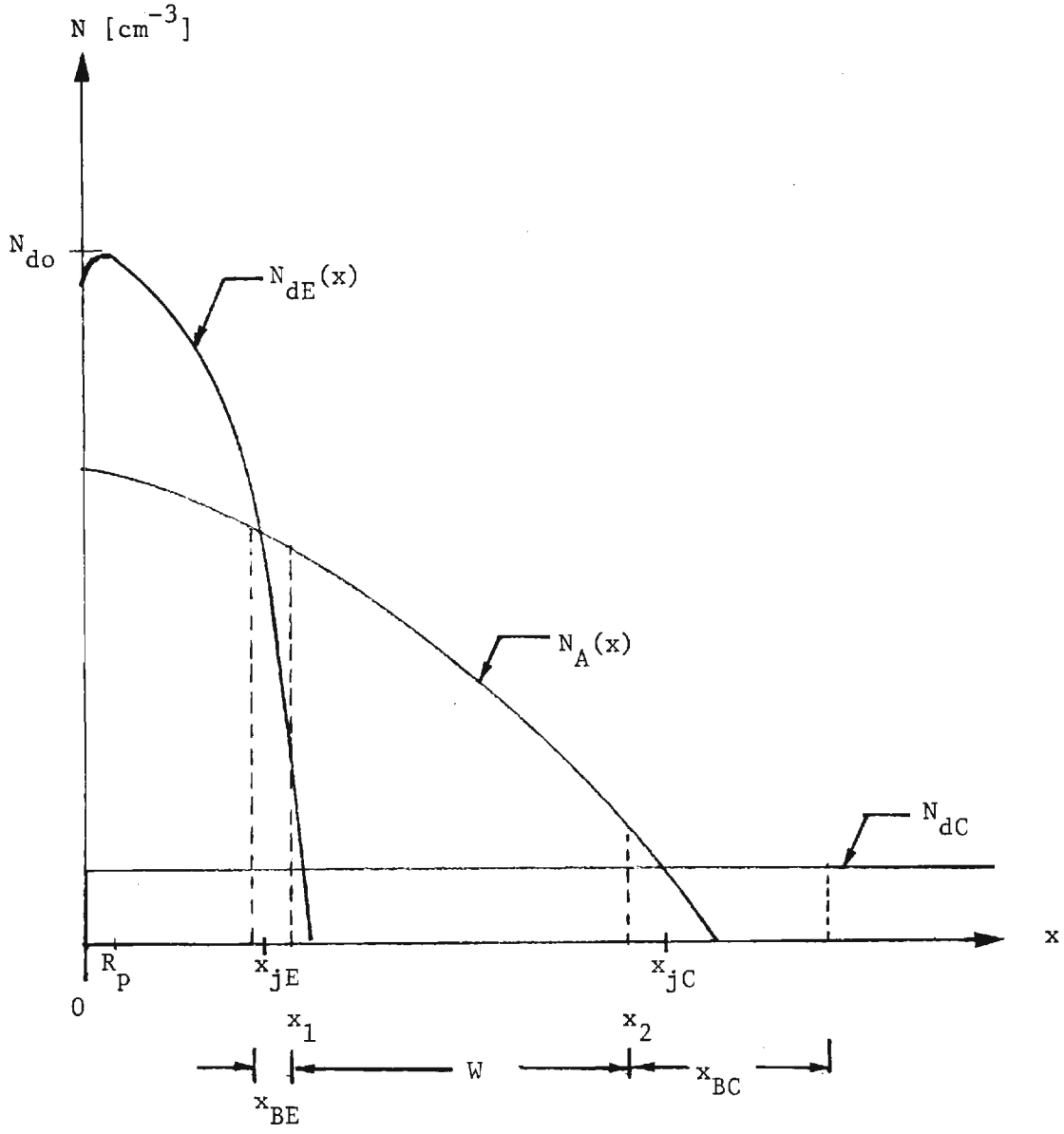


Figure 22

Bipolar Transistor Doping Profiles
Used to Analyze Gummel Number
Variations

in the base is given by

$$N_a(x) = N_A(x) - N_{dE}(x) - N_{dC} \qquad (7.1\text{-}5)$$

as the donors must be subtracted to account for dopant compensation. The Gummel number thus assumes the form

$$N_G = \int_{x_1}^{x_2} [N_{sA} e^{-x^2/d^2} - N_{do} e^{-(x-R_p)^2/2(\Delta R_p)^2} - N_{dC}] \, dx \qquad (7.1\text{-}6)$$

where x_1 and x_2 define the edges of the base quasi neutral region with $W=(x_2-x_1)$.

The junction depths x_{jE} and x_{jC} are found by searching for points of total dopant compensation. The base-emitter junction occurs where

$$N_A(x_{jE}) = N_{dE}(x_{jE}) + N_{dC} \; ; \qquad (7.1\text{-}7)$$

usually, the epitaxial doping is much smaller than either the base or emitter doping so that N_{dC} may be ignored. Using eqns. (7.1-3) and (7.1-4) then gives a quadratic equation for x_{jE} in the form

$$x_{jE}^2 \left[1 - \frac{d^2}{2(\Delta R_p)^2}\right] + \frac{x_{jE} d^2}{(\Delta R_p)} - \frac{R_p^2 d^2}{2(\Delta R_p)^2} \simeq d^2 \ln\left[\frac{N_{sA}}{N_{do}}\right] \qquad (7.1\text{-}8)$$

which may be solved for x_{jE}. The base-collector junction is found in a

similar manner using

$$N_A(x_{jC}) = N_{dE}(x_{jC}) + N_{dC}$$
$$\simeq N_{dC} \cdot \qquad (7.1\text{-}9)$$

This give the junction at

$$x_{jC} \simeq d\sqrt{\ln\left(\frac{N_{sA}}{N_{dC}}\right)} \cdot \qquad (7.1\text{-}10)$$

Once these are computed, the pn junction depletion widths x_{BE} and x_{BC} must be found. These, of course, are dependent upon the bias, with the most significant variation being in the base-collector junction (under forward-active bias). The analysis then gives values of $(x_p)_{BE}$ and $(x_p)_{BC}$ which represent the amount of depletion penetrating into the p-type base layer. Then,

$$x_1 = x_{jE} + (x_p)_{BE}$$
$$x_2 = x_{jC} - (x_p)_{BC} \qquad (7.1\text{-}11)$$

gives the limits of integration for the Gummel calculation.

The calculations outlined above are only approximate in that the doping profiles have been simplified to an extreme point. The analysis is, however, useful to understand the role that processing variations play in establishing ΔN_G.

Consider first the peak donor doping density N_{do} in the emitter

profile. This may be related to the implant dose D_I [cm^{-2}] by means of

$$N_{do} \simeq \frac{D_I}{\sqrt{2\pi}\ (\Delta R_p)} \quad . \qquad (7.1\text{-}12)$$

The dose is the most common measure of the ion implantation level. This equation demonstrates that variations in N_{do} are proportional to the measurement of D_I. The straggle (ΔR_p) is the standard deviation for the ion implant Gaussian, and is itself a statistical variable. Since N_{do} is inversely proportional to (ΔR_p) with the straggle typically being on the order of a few tenths of micron maximum, it is seen that the calculations are quite sensitive to the values obtained from the fabrication line measurements.

The acceptor magnitude N_{sA} is directly related to the thermal processing involved in the (assumed) base diffusion. This is seen by writing the familiar 2-step diffusion profile as

$$N_{sA} \simeq \frac{2N_o}{\pi} \sqrt{\frac{D_p t_p}{(Dt)_{eff}}} \qquad (7.1\text{-}13)$$

where N_o is the solid solubility of the dopant at the predeposit temperature, D_p the dopant diffusion coefficient at the predeposit temperatue, t_p the predeposit duration, and $(Dt)_{eff}$ the characteristic length associated with all of the thermal steps following the predeposit. Also,

$$d^2 = 4(Dt)_{eff} \quad , \qquad (7.1\text{-}14)$$

so that the diffusion parameters set all of the important acceptor profile quantities that are needed to compute the Gummel number.

This discussion shows that the processing variations in establishing the crucial base properties of the transistor are manifest in all stages of the Gummel number determination. Consequently, there is no simple manner in which ΔN_G can be computed with a reasonable confidence level. Owing to this fact, the most reliable method for obtaining information on Gummel number variations is to use empirical results extracted directly from the processing line under study. Then, the simplistic approach manifest in eqn. (7,1-2) can be used to obtain a first estimate of the variations.

7.2 Ideality Factor

The next quantity which will be analyzed is η_F, the forward current emission coefficient or ideality factor. The default SPICE value is unity, corresponding to an ideal behavior at the base-emitter junction. In the real world, this must be modified to account for recombination current in the base-emitter depletion region. Although this is the most important at low V_{BE} values, the exact number used to analyze a circuit can have a significant overall effect throughout the VTC range.

The simplest analysis of the depletion region recombination current gives the result that, in forward active bias,

$$I_E \simeq \frac{I'_S}{\alpha_F} e^{V_{BE}/V_T} + I_R e^{V_{BE}/2V_T} \qquad (7.2\text{-}1)$$

where

$$I_R \simeq \frac{qA_E n_i x_{BE}}{2\tau_o} \qquad (7.2\text{-}2)$$

gives the magnitude of the recombination current. τ_o is an effective lifetime such that

$$\tau_o \simeq \frac{1}{2}(\tau_n + \tau_p). \qquad (7.2\text{-}3)$$

The dependence of x_{BE} on V_{BE} makes this term quite sensitive to the amount of forward bias applied to the base-emitter junction. In addition, the extra factor of (1/2) in the exponential gives the variation which is accounted for by η_F .

The origins of the ideality factor is not well based theoretically, but arises from the desire to write I_E and I_C as simple functions of V_{BE}. In other words, the current in eqn. (7.2-1) is forced into the form

$$I_E = \frac{I_S}{\alpha_F} e^{V_{BE}/\eta_F V_T} \qquad (7.2\text{-}4)$$

which simplifies circuit analysis considerably. The change in the critical VTC parameters of the ECL OR/NOR gate is easily understood by noting that η_F is responsible for setting the shape of the transistor transfer curve.

Consequently, all voltages will reflect even small changes in the η_F value.

Owing to the fact that η_F is empirically based, the value of $\Delta\eta_F$ should be directly obtained from test structures on the wafer.

7.3 Emitter Area Variations

The value of ΔA_E which appears in eqn. (7-13) for $\Delta I_C/I_C$ represents differences in the emitter layout from the nominal dimensions. Letting

$$\ell = \text{Emitter Stripe Width}$$
$$h = \text{Effective Emitter Periphery} \qquad (7.3\text{-}1)$$

the nominal emitter area is simply $A_E = h\ell$. Generally, the frequency response needed for bipolar circuits stipulates that ℓ correspond to the minimum allowable linewidth permitted by the lithography. Since the saturation current is proportional to A_E, this will result in the condition that $\ell << h$. Owing to this fact, the most important variation contributing to ΔA_E will arise from linewidth variations which give $\Delta\ell$. Thus,

$$\Delta A_E \simeq h(\Delta\ell) \qquad (7.3\text{-}2)$$

so that

$$\frac{\Delta A_E}{A_E} \simeq \frac{\Delta\ell}{\ell} \qquad (7.3\text{-}3)$$

provides a simple relation for the first term in eqn. (7-13).

7.4 Temperature Variations

The only remaining term in eqn. (7-13) is that which accounts for thermal variations. This is based on the fact that the intrinsic density n_i is a strong function of temperature. It is expected that once the chip reaches it quiescent operating temperature, this term will stabilize out. In other words, this term affects the absolute performance of a circuit, but is not expected to produce much variation when compared with chip from other lots under the same operating condtions. This term will not be discussed further.

The analysis above shows that the simplistic equation of current flow given by (7-1) can be broken down into basic processing parameters which results in collector current variations as expressed in (7-13). The SPICE results are therefore explained by means of more tangible variables since the current to voltage translation is easily accomplished using the relations developed in Section 5.

It is not possible to extrapolate any simple design criteria for how the noise margin and critical VTC voltages are formed in the ECL circuit. However, the discussion demonstrates that a step-by-step check is plausible, and should be based on the measurement of test structures in a fabrication line.

7.5 Minimum Power Supply Constraints

It is possible to use the analysis to extrapolate information on the minimum allowable power supply level which is acceptable for the circuit. In the current context, this is $V_{CC,min}$, although the results can be extended to the more conventional bias case where $V_{CC}=0$ and $-V_{EE}$ is applied to desensitize the circuit.

Equation (7-13) may be applied to study the minimum acceptable power supply voltage value by noting from Fig. 13 that

$$V_{NOR} = V_{CC} - I_C R_C$$
$$V_{OR} = V_{CC} - I_{CR} R_C \qquad (7.5\text{-}1)$$

where

$$I_C + I_{CR} = \alpha_F I_{EE} \quad . \qquad (7.5\text{-}2)$$

The value of V_{OH} is obtained when the collector current is minimized with a value $I_{C,min}$. Then

$$V_{OH} = V_{CC} - I_{C,min} R_C \qquad (7.5\text{-}3)$$

provides a more realistic value for the output high level. The output low voltage occurs when the collector current reaches a value of $\alpha_F I_{EE}$ so that

$$V_{OL} = V_{CC} - \alpha_F I_{EE} R_C \quad . \qquad (7.5\text{-}4)$$

Since the collector current is now expressed as $(I_C + \Delta I_C)$, V_{OH} has a variation of

$$\Delta V_{OH} = - \Delta I_{C,min} R_C \qquad (7.5\text{-}5)$$

while

$$\Delta V_{OL} = - \alpha_F \Delta I_{EE} R_C$$

$$= - \Delta I_{C,max} R_C \quad . \qquad (7.5\text{-}6)$$

The logic swing of the circuit is now given by

$$V_\ell = (V_{OH} + \Delta V_{OH}) - (V_{OL} + \Delta V_{OL}) \qquad (7.5\text{-}7)$$

so that variations in the collector currents give

$$\Delta V_\ell = \Delta V_{OH} - \Delta V_{OL} \quad . \qquad (7.5\text{-}8)$$

The worst-case situation is where

$$\Delta V_\ell < 0 \qquad (7.5\text{-}9)$$

since this lowers the logic swing and thus reduces both NM_H and NM_L.

To understand this set of equations, note that a minimum V_ℓ will be required to maintain the switching performance of the circuit. This implies that one should set values for $V_{OH,min}$ and $V_{OL,max}$ such

that

$$V_{\ell,min} = V_{OH,min} - V_{OL,max} \qquad (7.5\text{-}10)$$

is the minimum acceptable output logic swing. Using (7.5-3) and (7.5-4) gives

$$V_{OH,min} = V_{CC} - I_{C,min}R_C - |\Delta I_{C,min}|R_C \qquad (7.5\text{-}11)$$

and

$$V_{OL,max} = V_{CC} - I_{C,max}R_C + |\Delta I_{C,max}|R_C \quad . \qquad (7.5\text{-}12)$$

Adding these two equations then gives

$$V_{CC} \geq \frac{1}{2}[(V_{OH,min} + V_{OL,max}) + (I_{C,min} + I_{C,max})\, R_C + (|\Delta I_{C,min}| - |\Delta I_{C,max}|)\, R_C\,] \qquad (7.5\text{-}13)$$

as the power supply constraint. When combined with eqn. (7-13) for ΔI_C, this allows for a direct estimate of the minimum value of V_{CC}.

Now recall that the ideal logic swing for and ECL switch is given by

$$V_\ell = \alpha_F I_{EE} R_C \quad . \qquad (7.5\text{-}14)$$

Again using equations (7.5-3) and (7.5-4) gives the best-case realistic value of

$$V_\ell = (I_{C,max} - I_{C,min})R_C \qquad (7.5\text{-}15)$$

which is smaller than the ideal value. The limitations on the actual V_{CC} used to power the circuit can be studied in a slightly different approach which illustrates the interplay among the device and circuit parameters.

To extract the desired information, first note that $I_{C,max}$ occurs when $V_{in}=V_{OH}$ so that

$$I_{C,max} \simeq I_S \, e^{(V_{CC} - I_{C,min}R_C - V_E)/\eta_F V_T} \, . \qquad (7.5\text{-}16)$$

Similarly,

$$I_{C,min} \simeq I_S \, e^{(V_{CC} - I_{C,max}R_C - V_E)/\eta_F V_T} \qquad (7.5\text{-}17)$$

to this order of approximation. Combining these equations gives

$$V_\ell \simeq I_S R_C \, e^{(V_{CC}-V_E)/\eta_F V_T} \left[e^{-I_{C,min}R_C/\eta_F V_T} - e^{-I_{C,max}R_C/\eta_F V_T} \right] . \qquad (7.5\text{-}18)$$

Introducing the logic swing collector current

$$I_\ell = I_{C,max} - I_{C,min} \qquad (7.5\text{-}19)$$

and rearranging then yields the expression

$$V_{CC} = \eta_F V_T (V_E + I_{C,max} R_C - \frac{1}{2} I_\ell R_C) \times \ln \left[\frac{V_\ell}{2 I_S R_C \sinh(\frac{I_\ell R_C}{2 \eta_F V_T})} \right] , \qquad (7.5\text{-}20)$$

This provides the relation between V_{CC} and the desired logic swing, and also incorporates the important transistor parameters I_S and η_F. As a final point, it should be noted that the value of the collector resistance R_C is generally a quantity which exhibits great variations from lot-to-lot. Consequently, this should be accounted for in the analysis by means of the standard ratio $(\Delta R_C / R_C)$.

The discussion in this entire chapter is applicable to off-chip driver analysis, so that this specific topic is not detailed here.

8. Basic Charge-Control Description

During the initial phases of the research it was thought that an analytic charge-control model would be the best approach for modelling ECL VTC variations. The work in this section deals with such an effort, and presents the basic calculations needed to model the transient switching in the circuit. As will be seen during the discussion, the charge-control approach is quite messy, and that it is difficult to draw conclusions from the equations. However, the work does provide for an initial starting point which has much potential in the future.

The starting point of the calculations is to write the forward-active collector current from eqn. (3.2-1) in the form

$$i_C \simeq \frac{Q_F}{\tau_F} - \frac{dQ_{VC}}{dt} \qquad (8\text{-}1)$$

which assumes that the reverse charges are negligible. Using eqns. (3.2-2) and (3.2-3) together with the definiton of I_S in eqn. (7-6) allows one to write

$$i_C \simeq \frac{q^2 A_E^2 n_i^2 \tilde{D}_n}{I_S \tau_F} e^{V_{BE}/V_T} - \frac{dQ_{VC}}{dt} . \qquad (8\text{-}2)$$

To analyze the ECL switching, it is necessary to approximate the base-collector depletion charge Q_{VC}. A reasonable first approximation is to assume a linearly graded pn junction such that

$$N_d - N_a = a\, x \qquad (8\text{-}3)$$

with a the grading constant. To work this into the analysis, first write

$$\frac{dQ_{VC}}{dt} = \frac{dQ_{VC}}{dW} \frac{dW}{dV_{BC}} \frac{dV_{BC}}{dt} \qquad (8\text{-}4)$$

where W is again the quasi-neutral base width. Now, a change in the base-collector voltage V_{BC} will induce a change in the base-collector depletion width x_{BC}. Since W is directly dependent upon x_{BC} [as demonstrated in equations (7.1-11)], the time rate of change for the depletion charge may be rewritten as

$$\frac{dQ_{VC}}{dt} \simeq \frac{dQ_{VC}}{dx_{BC}} \frac{dx_{BC}}{dV_{BC}} \frac{dV_{BC}}{dt} \quad . \qquad (8\text{-}5)$$

Now then, the linearly graded profile gives directly a depletion charge of

$$Q_{VC} \simeq qA_C \frac{ax_{BC}^2}{4} \qquad (8\text{-}6)$$

so that

$$\frac{dQ_{VC}}{dx_{BC}} \simeq \frac{1}{2} q A_C a x_{BC} \quad . \qquad (8\text{-}7)$$

The second factor in (8-5) can be related to the forward Early Voltage V_{AF} which is defined by

$$\frac{dW}{dV_{BC}} = \frac{N_G}{N_a(W)\ V_{AF}} \simeq \frac{dx_{BC}}{dV_{BC}} \quad . \tag{8-8}$$

Equation (8-5) is thus reduced to

$$\frac{dQ_{VC}}{dt} \simeq \frac{\frac{1}{2}\ qa\ A_C\ x_{BC}}{\left[\frac{N_G}{N_a(W)\ V_{AF}}\right]} \left(\frac{dV_{BC}}{dt}\right) \tag{8-9}$$

so that the collector current equation assumes the form

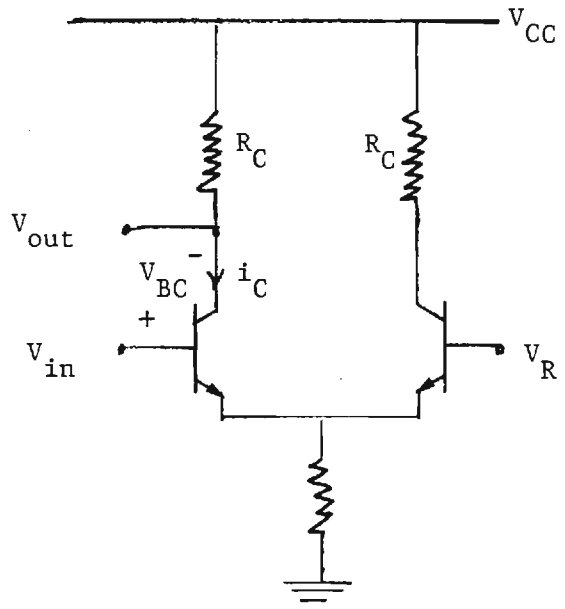
$$i_C \simeq \frac{q^2 A_E^2\ n_i^2\ D_n}{I_{S\ F}}\ e^{V_{BE}/V_T} - \frac{qax_{BC}A_C\ N_G}{2V_{AF}N_a(W)} \frac{dV_{BC}}{dt} \quad , \tag{8-10}$$

This may be considered a basic differential equation which gives the transient current.

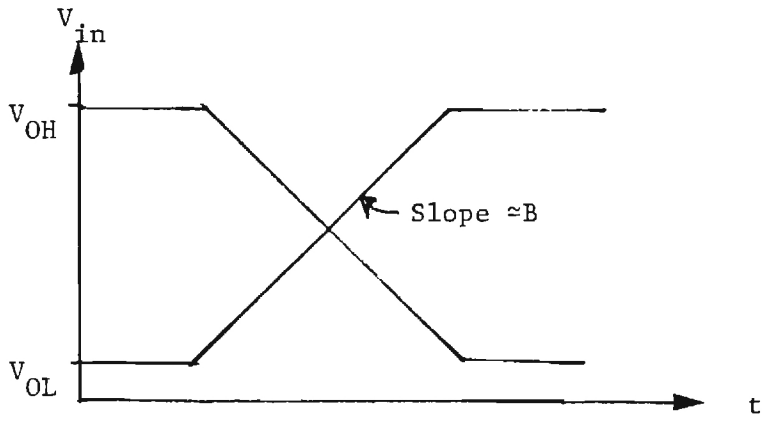
In order to show how the above equation can be used to describe the circuit switching, suppose that the input voltage $V_{in}(t)$ in the ECL configuration is modelled by the waveform shown in Fig. 23. In Fig. 23(a), it is seen that

$$\frac{dV_{BC}}{dt} = \frac{d(V_{in}-V_{out})}{dt} \quad , \tag{8-11}$$

Modelling the input voltage during the transition as having a linear



ECL Switch
(a)



Simplified Input Waveform
(b)

Figure 23

ECL Charge-Control Modelling

ramp with slope B as shown in Fig. 23(b) then gives

$$\frac{dV_{BC}}{dt} \simeq \frac{d(Bt - V_{out})}{dt} \quad . \tag{8-12}$$

Since

$$V_{out} = V_{CC} - i_C R_C \tag{8-13}$$

this yields

$$\frac{dV_{BC}}{dt} \simeq B + R_C \frac{di_C}{dt} \quad . \tag{8-14}$$

Substituting into the right hand side of eqn. (8-10) finally gives the current equation

$$i_C \simeq \frac{q^2 A_E^2 n_i^2 \tilde{D}_n}{I_S \tau_F} e^{V_{BE}/V_T} - \frac{qaA_C W N_G x_{BC}}{2V_{AF} N_a(W)} \left(B + R_C \frac{di_C}{dt}\right). \tag{8-15}$$

This may be rewritten as

$$\frac{di_C}{dt} + \frac{2A_E^2 N_a(W)\, V_{AF}}{qA_C\, N_G x_{BC} R_C a}\, i_C(t) \simeq \frac{2N_a(W)V_{AF}}{x_{BC} R_C\, a} \left[\frac{e^{V_{BE}/V_T}}{\tau_F} - \frac{x_{BC} aB}{N_a(W) V_{AF}}\right], \tag{8-17}$$

This is a linear ordinary differential equation which may be solved by

standard techniques. The solution is found to be

$$i_C(t) \simeq qA_E N_G \left[\frac{2\, N_a[W(t)]\, V_{AF} V_T\, e^{[V_{in}(t)-V_E]/V_T}}{\tau_F(qaBA_E N_G x_{BC}(t) R_C + 2N_a[W(t)]\, V_{AF}\, V_T)} - \frac{aBx_{BC}(t)}{2N_a[W(t)]\, V_{AF}} \right] \qquad (8\text{-}18)$$

which descibes the current during the input transition ramp. It is seen that the charge-control solution to the problem results in expression which are quite cumbersome to work with. Although some simplistic interpretations are possible, these discussions are not as fruitful when compared to the analysis in Section 7. Consequently, the analysis of the charge-control results will not be discussed further.

9. VTC Dependence on FanOut (FO)

The SPICE program was also used to investigate the changes in critical VTC points as a function of the FanOut (FO). The basic circuit employed in the analysis in illustrated in Fig. 24 which defines the "internal" ("I" subscripted) and "external" ("E" subscripted) variables . The basic FO=n is used in the analytic discussion, while the SPICE run tended to look at FO=3.

A representative sampling of SPICE results are shown in Figs. 26 -29. Figure 26 deals with the changes in the VTC levels as a function of the number of inputs driven; a FO of 3 was assumed. Figure 25 summarizes the results of the SPICE calculations for FO values from 0 to 5. The dependence on the FO value is particularly striking, and is the subject of the analysis later in the section.

Figure 27 shows the variations induced by having unequal R_C values; this is the realistic case.

Figure 28 is directed towards the voltage level changes with η_F for a FanOut of 3. A similar set of plots is provided in Fig. 29 for variations which are induced by I_S. These two plots of are particular interest since they extend the results of the Section 7 to the case for a realistic FanOut value.

The results obtained from the SPICE simulations can be compared to the analytic calculations with good results. In order to derive the various equations, the circuit parameters defined in Fig. 24 will be referenced for notational purposes.

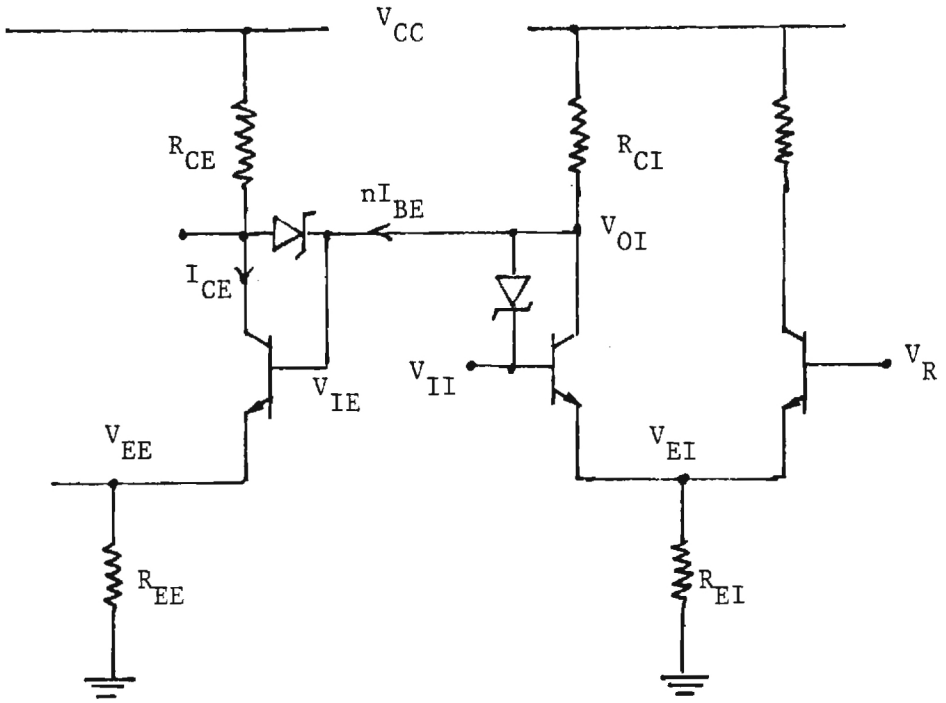


Figure 24

Circuit Used for FanOut FO=n Calculation

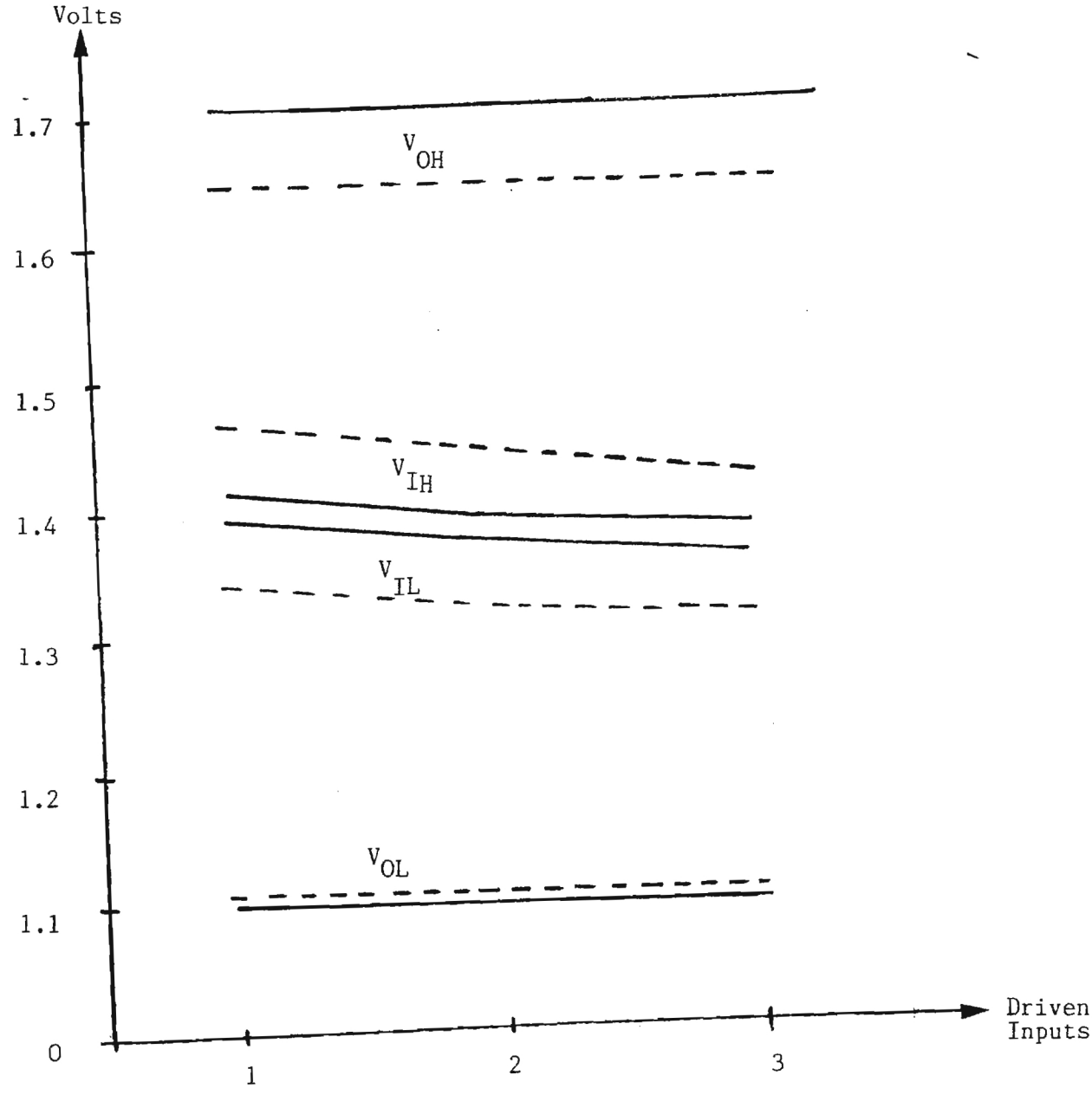


Fig. 26

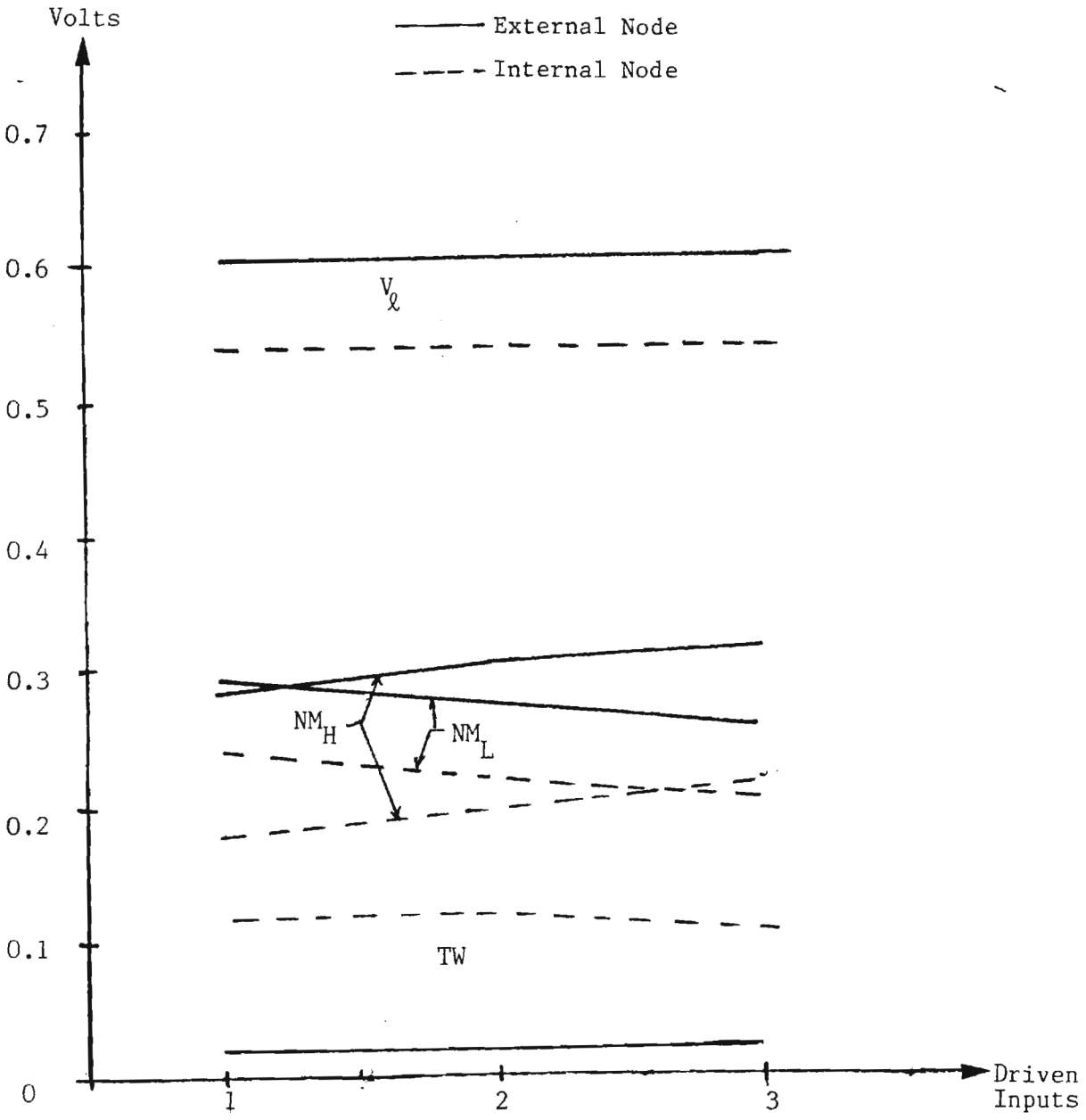


Figure 26

VTC Dependence on the Number of Driven Inputs

FO =3, 0.1 Ω Interconnect

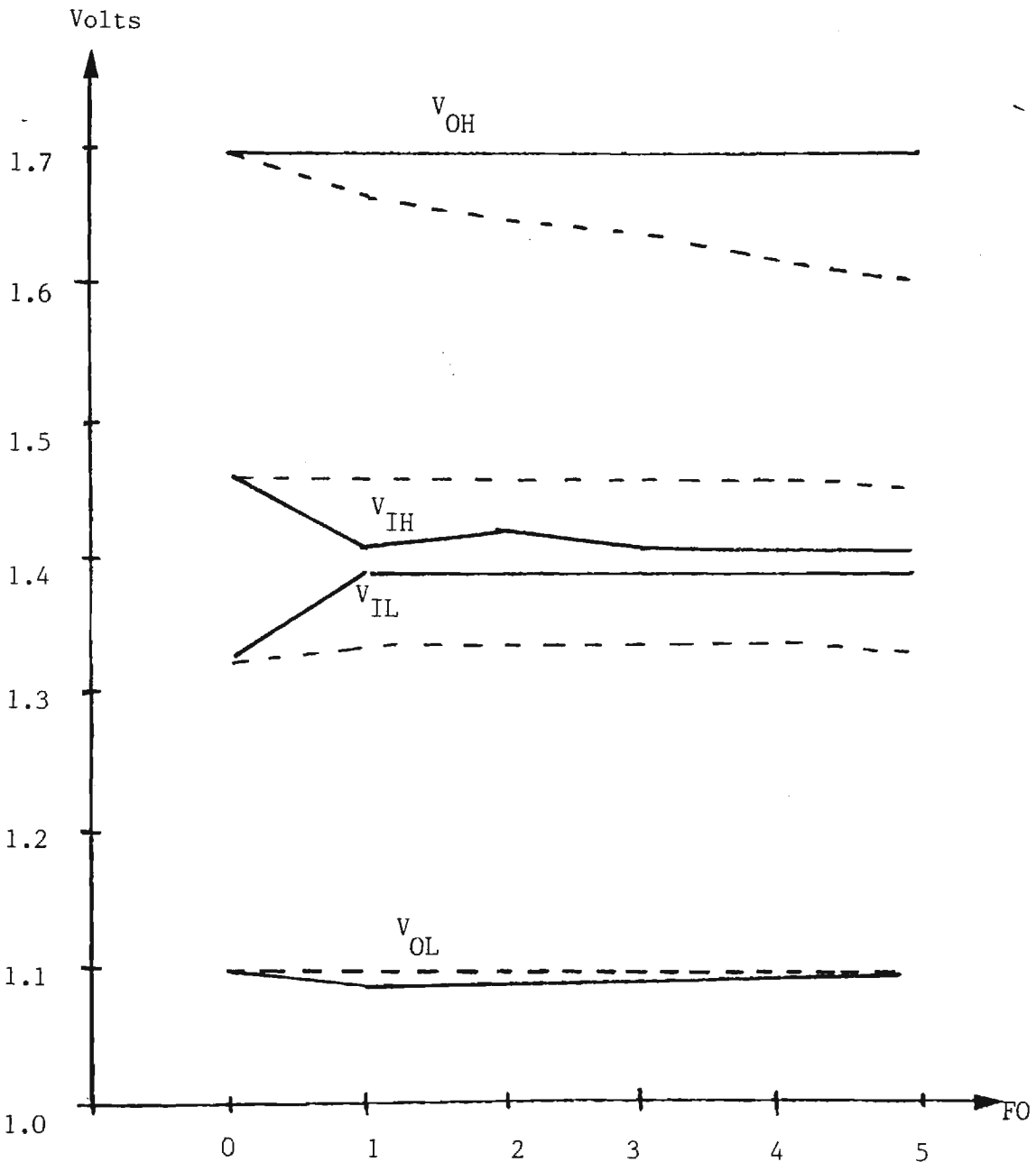


Fig. 25

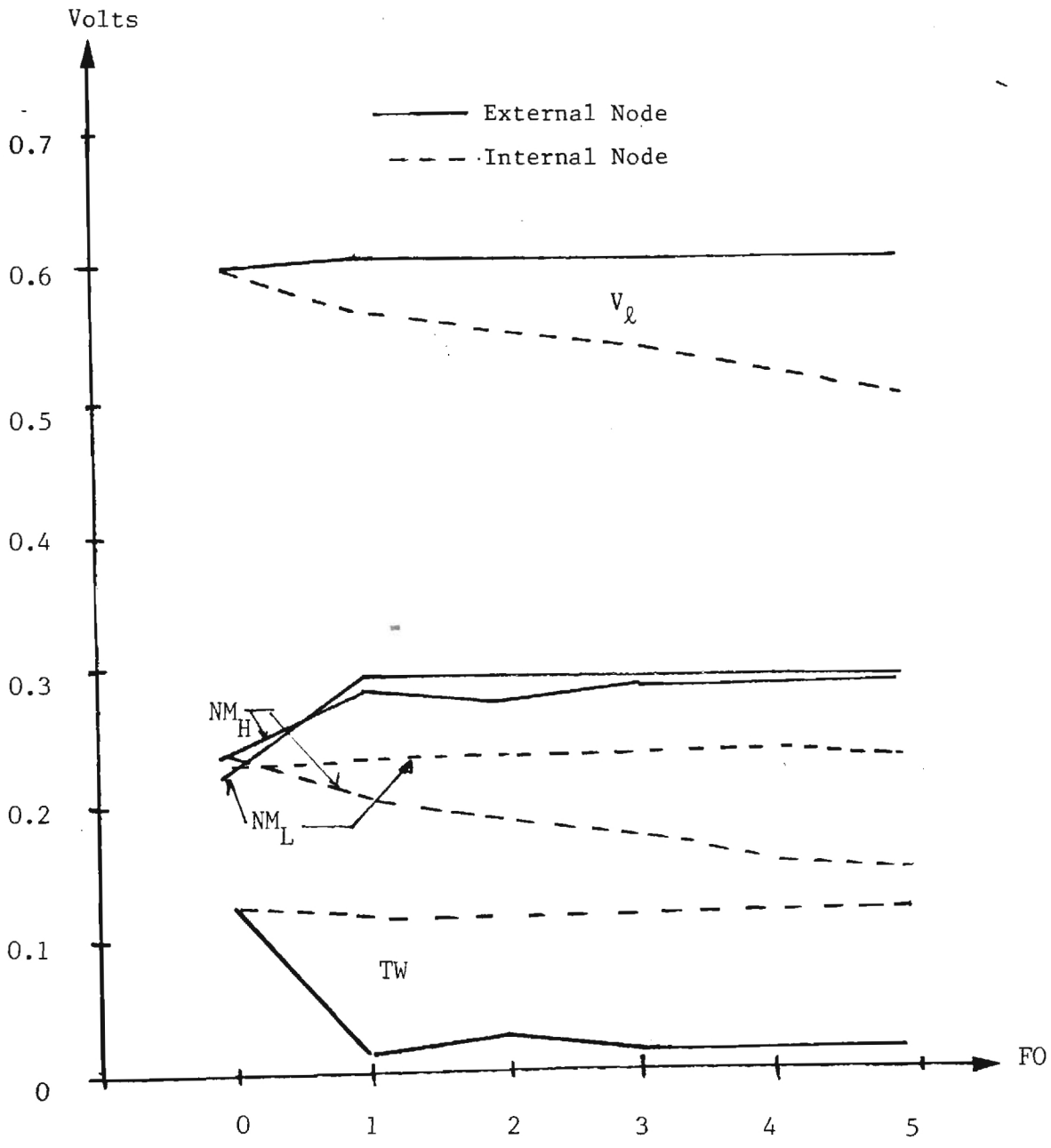


Figure 25

VTC Dependence on FanOut (FO)

1 Input Driven, 0.1 Ω Interconnect

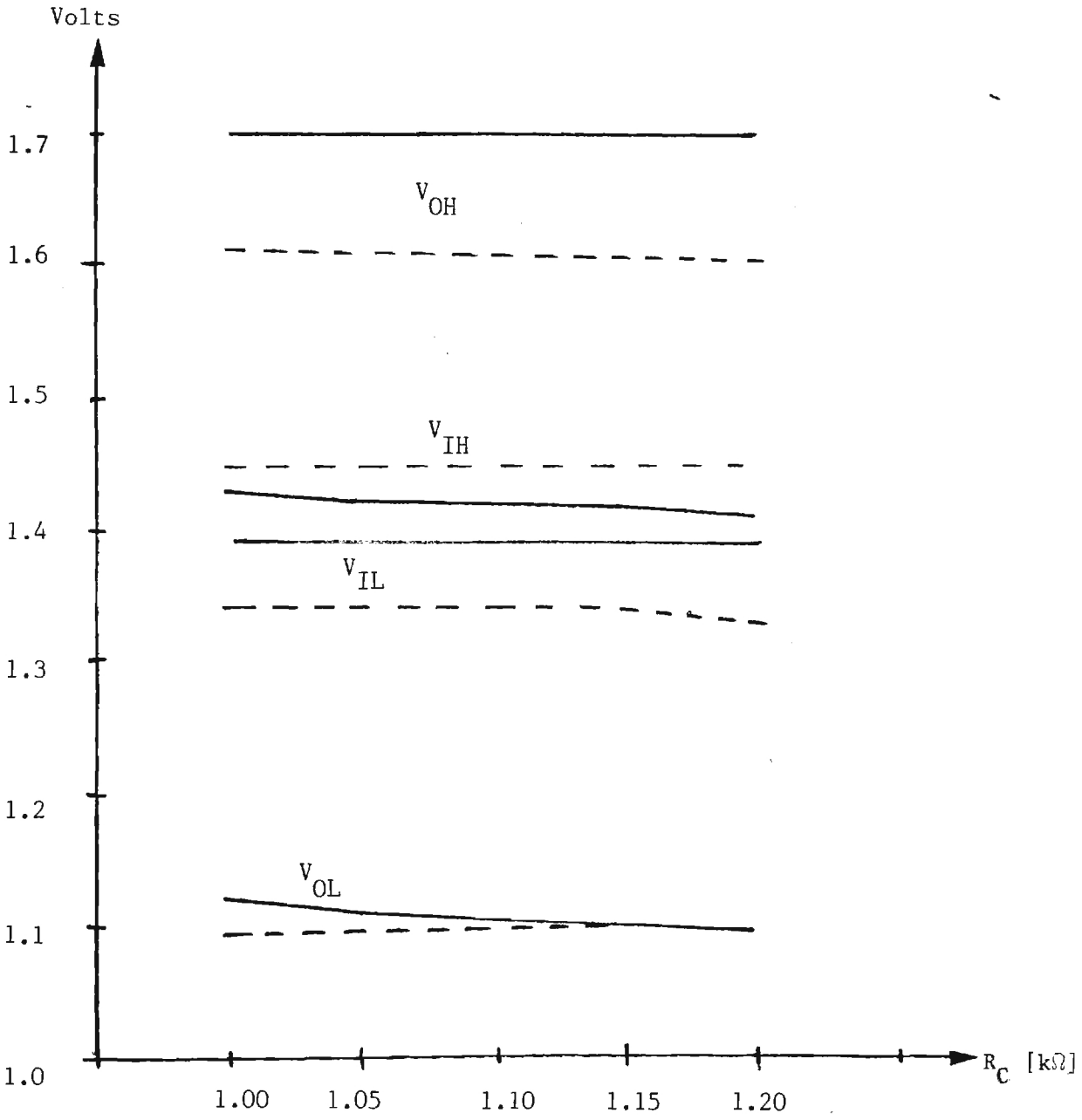

Volts
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
V_{OH}
V_{IH}
V_{IL}
V_{OL}
1.00
1.05
1.10
1.15
1.20
R_C [kΩ]

Fig. 27

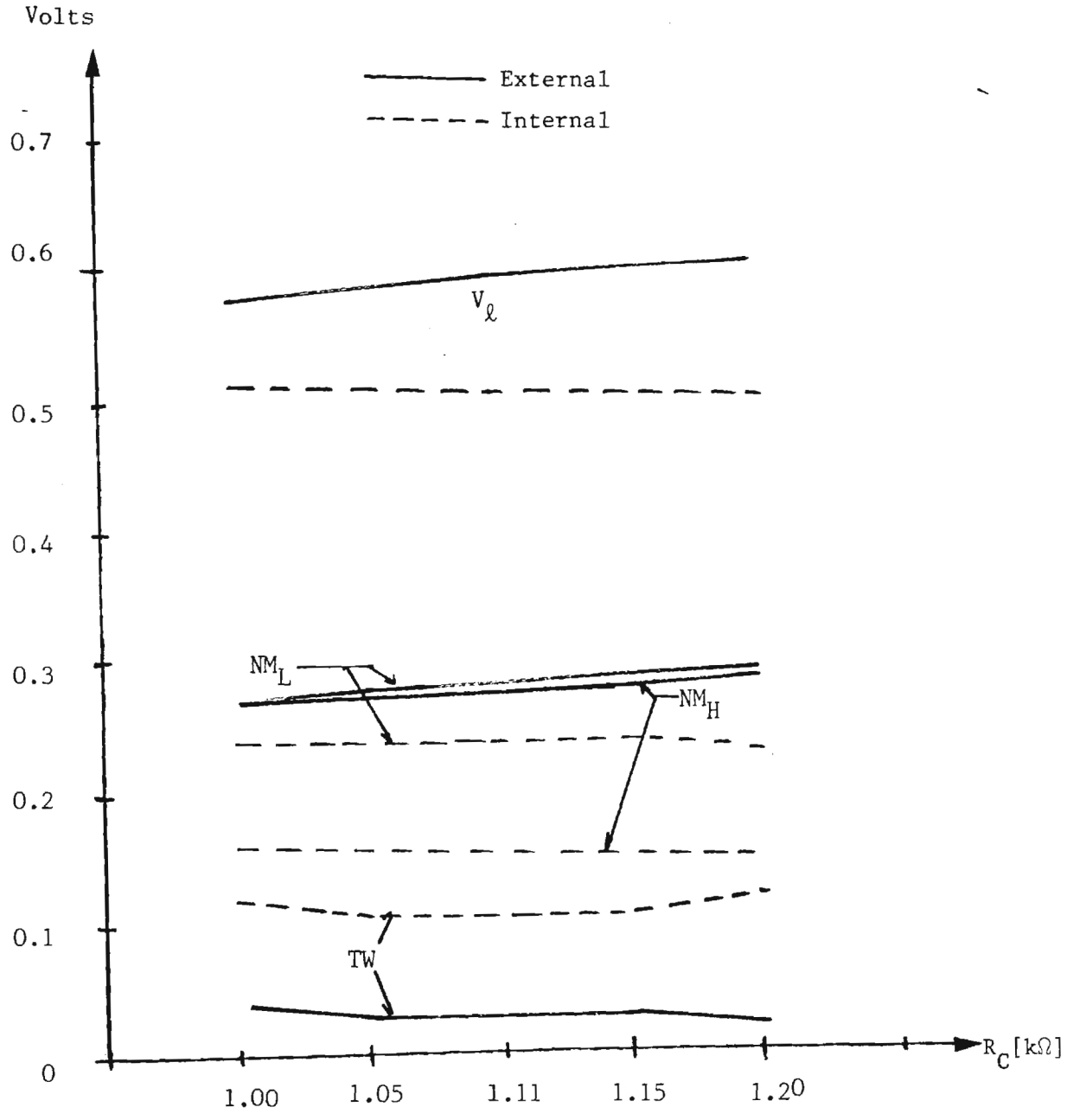


Figure 27

VTC Changes from Unbalanced R_C

FO=5, 0.1 Ω Interconnects

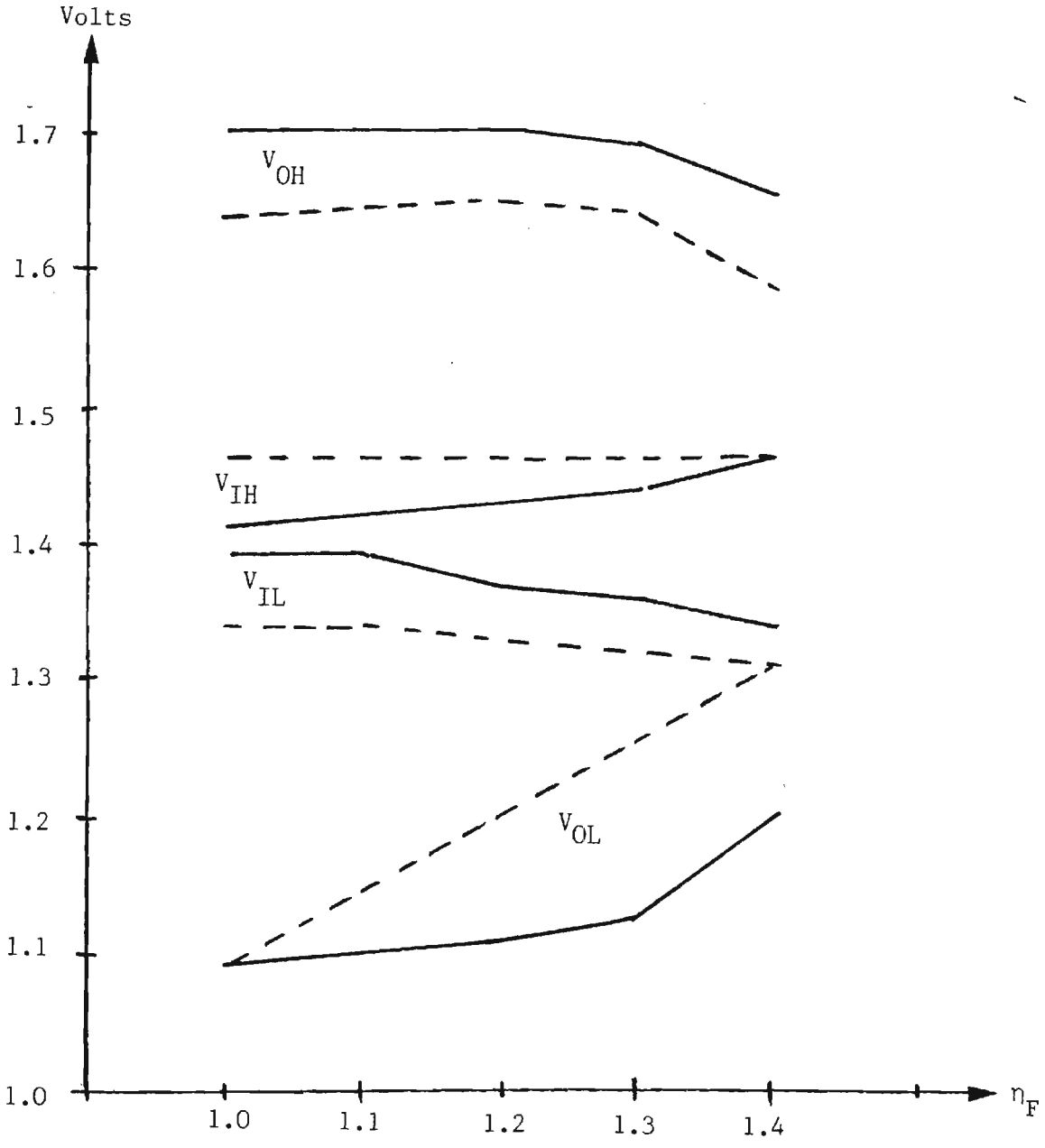


Fig. 28

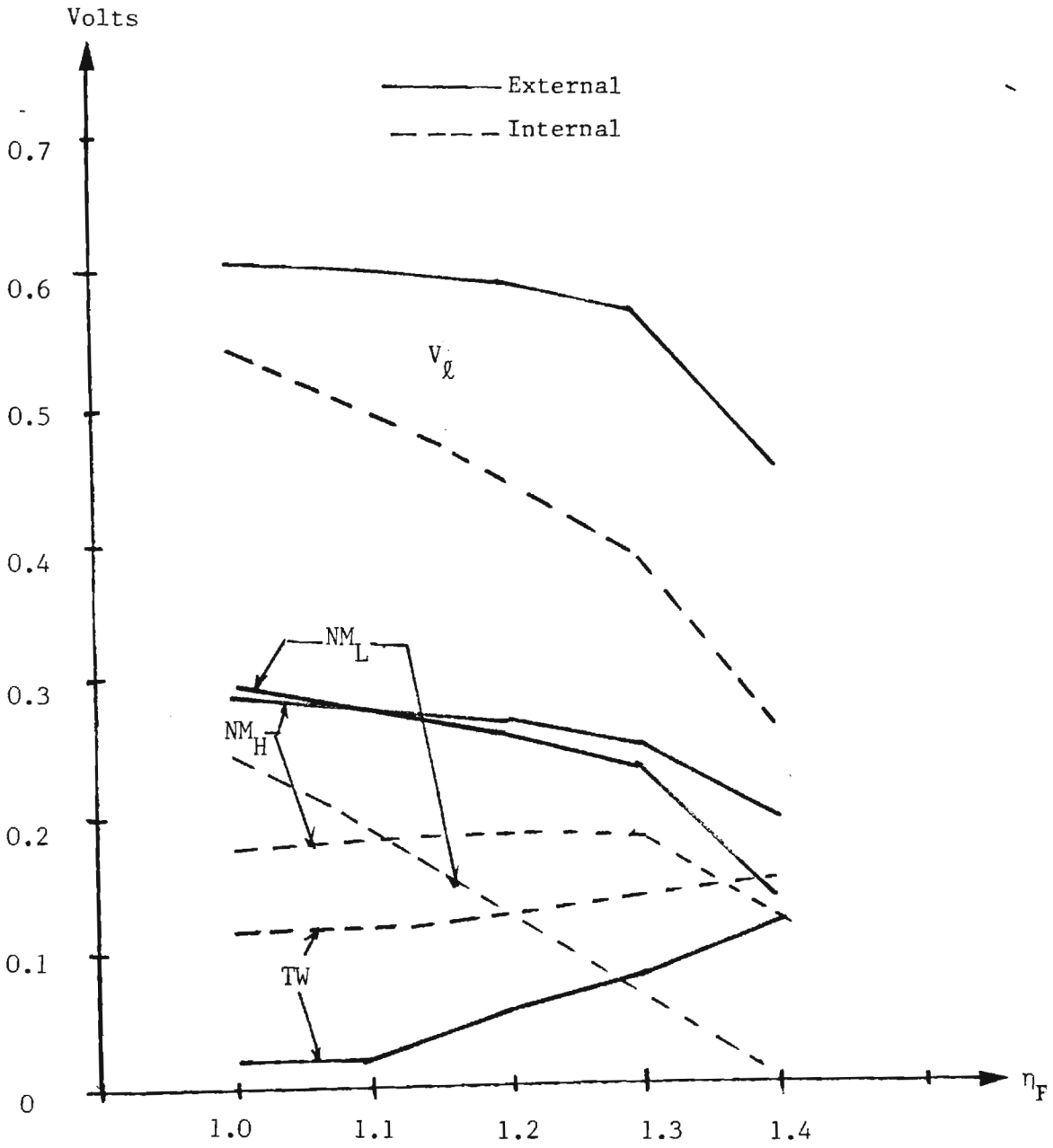


Figure 28

VTC Changes from η_F with FO=3

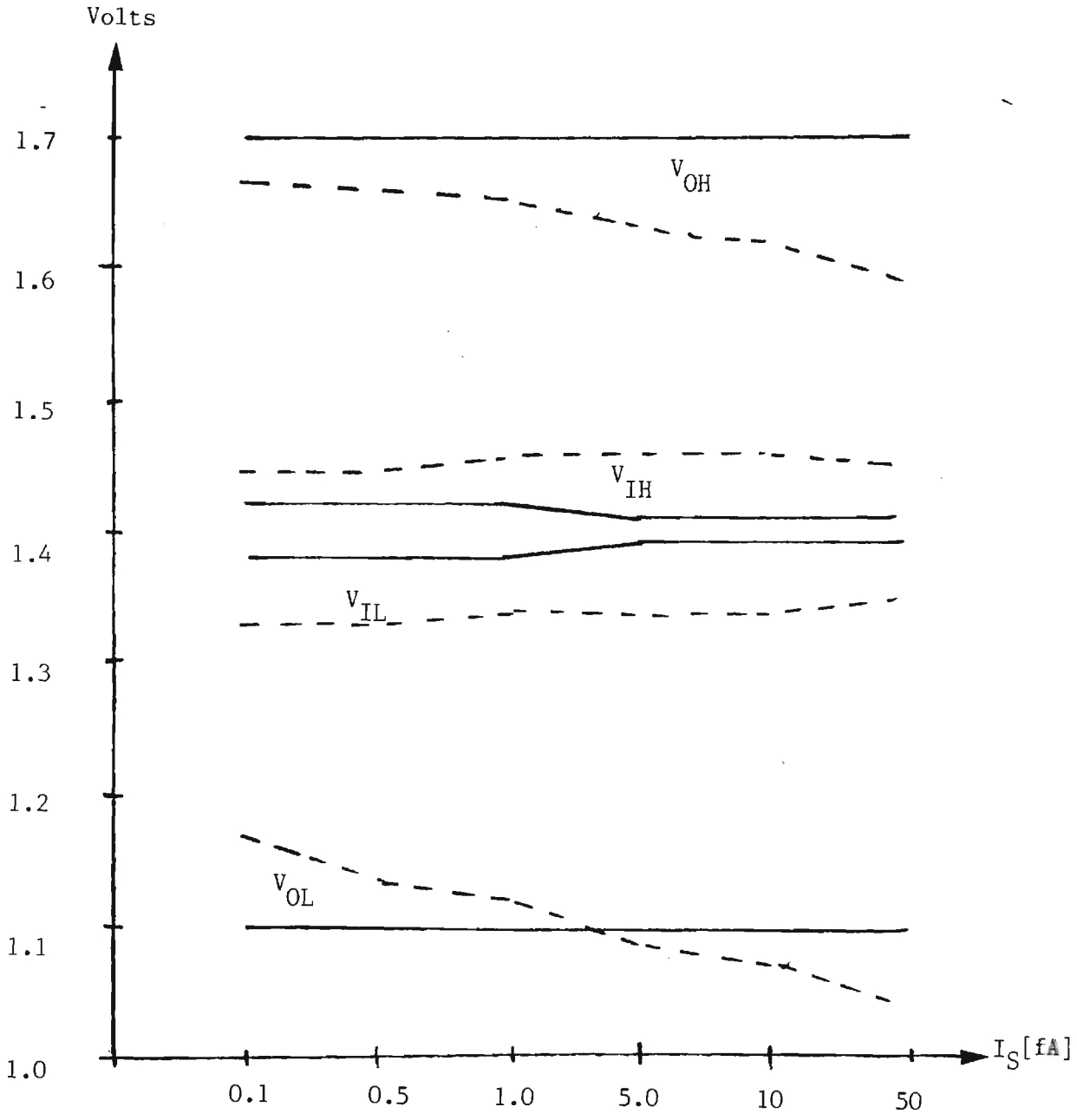


Fig. 29

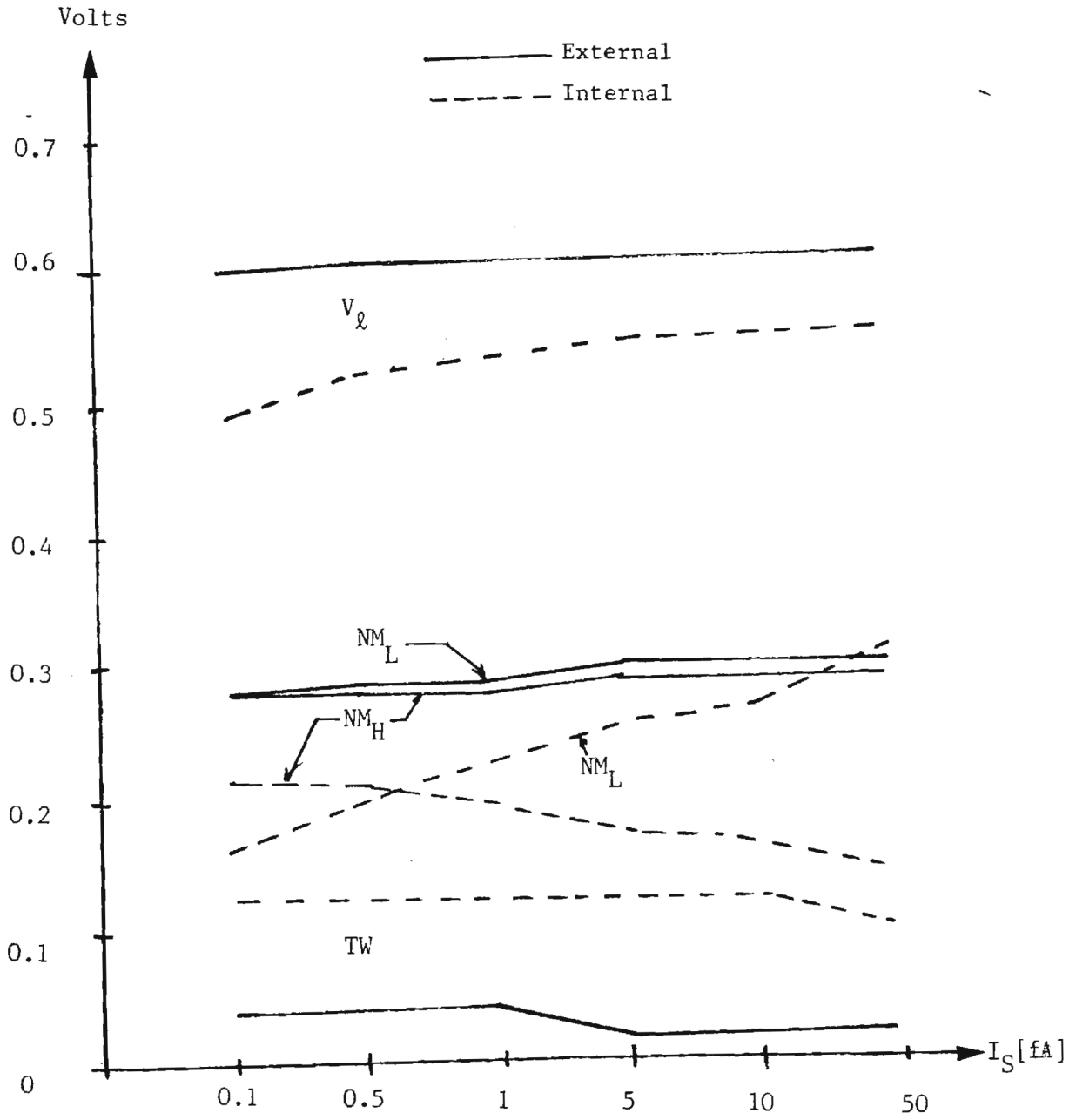


Figure 29

VTC Variation with I_S for FO=3

Consider first the calculation of V_{OHI}. By inspection,

$$V_{OHI} = V_{CC} - I_R R_{CI} = V_{CC} - I_{CI} R_{CI} - \frac{n I_{CE} R_{CI}}{\beta_{FE}} \quad . \qquad (9\text{-}1)$$

Assuming that I_{CI} is small then gives

$$V_{OHI} \simeq V_{CC} - R_{CI}\left[I_{COI} + \frac{n I_{SE}}{\beta_{FE}} e^{V_{on,E}/V_T}\right] \quad . \qquad (9\text{-}2)$$

For the external node, it is found that

$$V_{OHE} \simeq V_{CC} - I_{SE} R_{CE} e^{(V_{OLI} + V_{on,E} - V_R)/V_T} \qquad (9\text{-}3)$$

provides the output high voltage.

The value of V_{OLI} is obtained from writing

$$V_{OLI} \simeq V_{CC} - I_{SI} R_{CI} e^{V_{on,E}/V_T} \qquad (9\text{-}4)$$

which may be rewritten as

$$V_{OLI} \simeq V_{CC} - R_{CI}\left[I_{SI} e^{V_{on,I}/V_T} + \frac{n I_{SE}}{FE} e^{(V_{OLI} + V_{on,E} - V_R)/V_T}\right] . \qquad (9\text{-}5)$$

This is actually a transcendental equation, since V_{OLI} appears on both sides. The equivalent external value is much simpler and is

$$V_{OLE} = V_{CC} - I_{SE} R_{CE} e^{V_{on,E}/V_T} \quad . \qquad (9\text{-}6)$$

The calculation of V_{IHI} proceeds by writing

$$V_{OI} = 0.1(V_{OHI} - V_{OLI}) + V_{OLI}$$
$$= V_{CC} - I_{SI}R_{CI}\, e^{V_{BEI}/V_T} \qquad (9\text{-}7)$$

as the output voltage. V_{IHI} occurs for

$$V_{BEI}=V_T \ln \left[\frac{V_{CC} - [nR_{CI}I_{SE}/\beta_{FE}]e^{[0.1(V_{OHI}-V_{OLI}) + V_{on,E}-V_R]/V_T}}{I_{SI}R_{CI}} \right] . \qquad (9\text{-}8)$$

The analogous external value is obtained from solving

$$V_{CC}-I_{SE}R_{CE}e^{V_{BEE}/V_T} = 0.1(V_{OHE}-V_{OLE}) + V_{OLE}=V_{OE} \qquad (9\text{-}9)$$

in conjunction with

$$V_{BEE}= V_T \ln \left[\frac{V_{CC} - 0.1\,(V_{OHE}- V_{OLE}) - V_{OLE}}{I_{SE}R_{CE}} \right] . \qquad (9\text{-}10)$$

The last equations which need to be stated are those for V_{IL}. For the internal parameter V_{ILI}, the basic equation is

$$V_{OI} = V_{CC}-T_RR_{CI} = V_{CC}- \frac{nI_{SE}R_{CI}}{\beta_{FE}} e^{V_{on,E}/V_T} - I_{SI}R_{CI}e^{V_{BEI}/V_T} \qquad (9\text{-}11)$$

with V_{ILI} occuring when

$$V_{ILI}=V_R - V_{on,I} + V_T \ln \left[\frac{V_{CC} - \frac{nI_{SE}R_{CI}}{\beta_{FE}} e^{V_{on,E}/V_T} - 0.9(V_{OHI}-V_{OLI}) - V_{OLI}}{I_{SI}R_{CI}} \right] . \quad (9\text{-}12)$$

Finally,

$$V_{ILE}=V_R - V_{on.E} + V_T \ln \left[\frac{V_{CC} - 0.9(V_{OHE}-V_{OLE}) - V_{OLE}}{I_{SE}R_{CE}} \right] \quad (9\text{-}13)$$

provides the last required equation.

Although the equations may seem a bit messy at first sight, they are all straightforward to use. The most important point about the analysis is the fact that the numbers computed using these equations are extremely close to the SPICE results. As a means of comparison, for SPICE parameters of I_S= 3 [fA], r_C = 1200 [Ω], β_F=80 and V_{on}=0.7 [V], the following chart can be easily verified:

FO (n)	V_{OHI}	
	Computed	SPICE
0	1.70	1.70
1	1.678	1.670
2	1.656	1.650
3	1.633	1.640
4	1.611	1.618
5	1.589	1.600

The closeness of the numbers shows that the analytic treatment is a

a good basis for predicting the performance of the ECL logic gates under varying FanOut numbers.

It is seen by inspection that no generalized trend is obvious in the performance of the gate with regards to the parameters varied in this section. Owing to this, it is not possible to state simplistic design criteria. Rather, the noise margin formation requires a complete calculation based on the circuit properties.

10. Chip Level Influences on the VTC

This chapter will be directed towards the study of chip-level coupling be means of parasitic capacitances which exist because of overlapping interconnect levels. A simplistic view of the problem is illustrated in Fig. 30. It is seen that the 1st layer interconnect material is used to couple the output of Stage 1 to its destination, and also serves to feed the input of stage 2, Owing to the presence of the 2nd level interconnect shown, a parasitic coupling capacitance structure will be formed which could conceivably cause gate-to-gate coupling problems. The most severe example would be where swtiching Stage 1 would induce Stage 2 to switch.

The overlap of the two interconnect layers is shown in Fig. 31. This is the cross-section as seen along the line A-A' in the previous drawing. Assuming that the insulator has a permittivity ε_{ox} (e.g, SiO_2), then it is possible to define three parasitic unit-area capacitances:

$$C_1' = \frac{\varepsilon_{ox}}{d_1} \qquad [F/cm^2]$$

$$C_2' = \frac{\varepsilon_{ox}}{d_2} \qquad [F/cm^2]$$

$$C' = \frac{\varepsilon_{ox}}{d} \qquad [F/cm^2] \quad . \qquad (10\text{-}1)$$

C_2' describes the coupling between level 1 and level 2 interconnect layers, C_1' is the absolute level 1 to substrate capacitance, and C' is the level 2 to substrate capacitance. The actual capacitance for

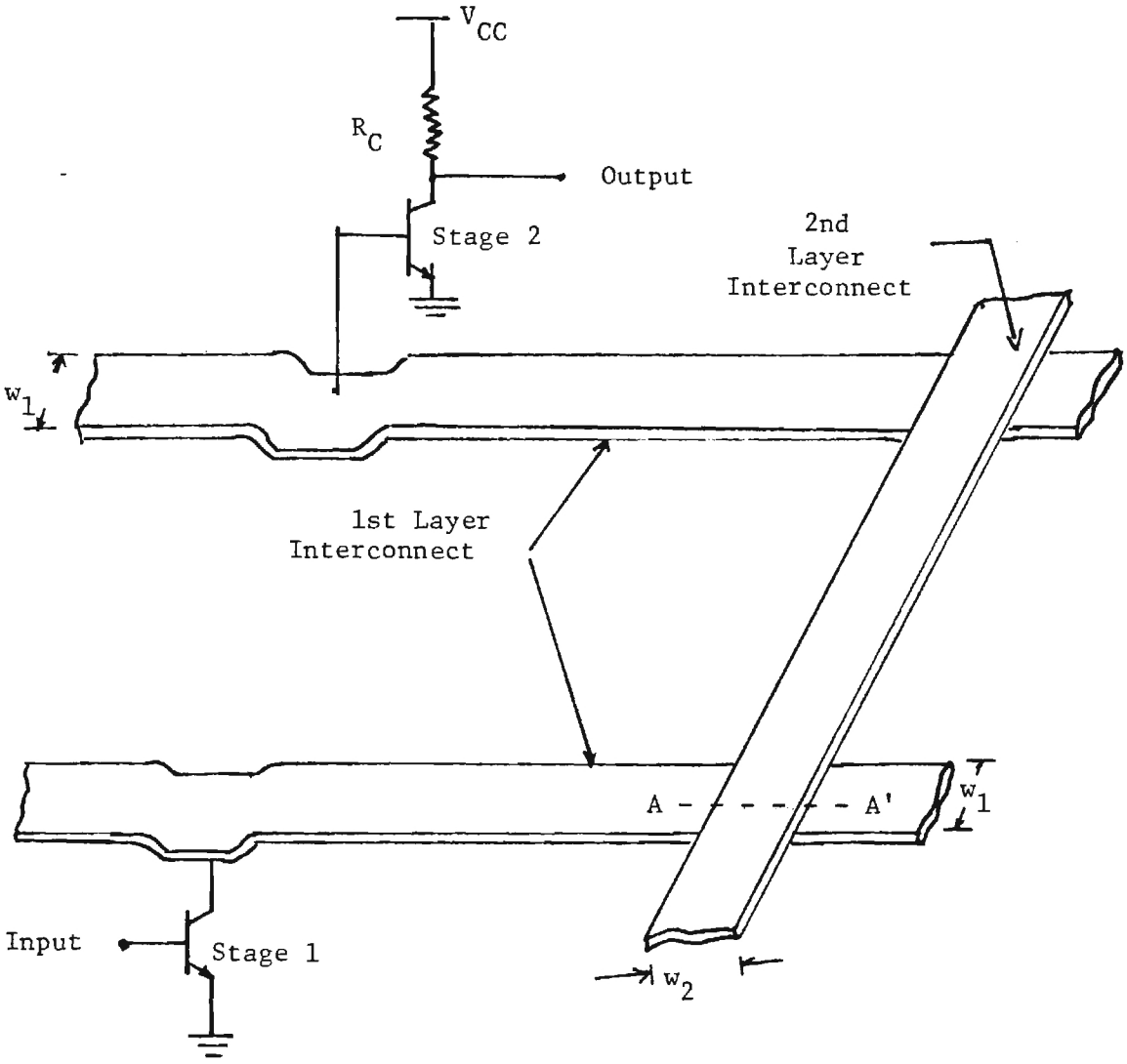


Figure 30

Simplified Interconnect
Coupling Problem

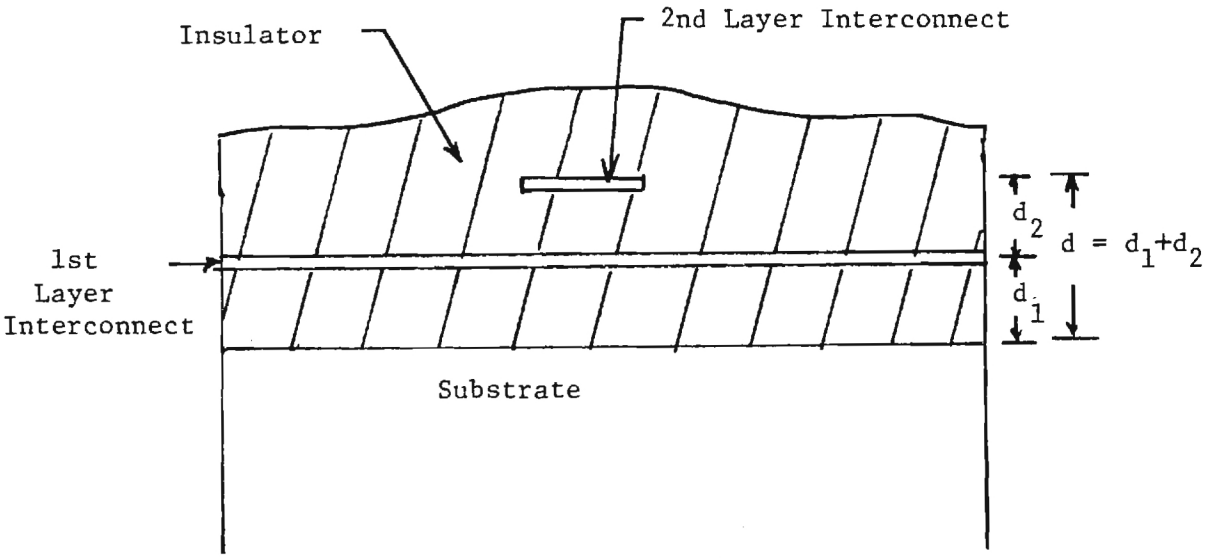


Figure 31

Overlap Capacitance Between
Interconnect Layers

circuit calculations is obtained by multiplying these quantities by appropriate areas.

The problem illustrated in Fig. 30 is modelled with the transmission line equivalent shown in Fig. 32. This simplified structure models the interaction between the two logic stages by means of the interaction points denoted by (A) and (B) in the drawing. The problem discussed here is where a voltage wavefront V_1 is introduced onto the line such that it can propagate a distance ℓ_1 to the point A. Here the wavefront is capacitively coupled onto the 2nd level interconnect line, where it propagates a distance ℓ_2 and hits interaction point B. The final path is where the signal is coupled back to interconnect level 1 and then travels a distance ℓ_2 to induce the voltage V_2 at the input of Stage 2.

Owing to the transmission line modelling, the actual solution to the problem is dependent upon the voltage wavelength λ. This allows the problem to be broken up into two calculations, one for a large wavelength and the other for the case where λ is on the order of the circuit dimensions.

The simplest of these is the case where

$$\lambda >> \text{Chip Dimensions} \qquad (10\text{-}2)$$

since in this limit the lines degenerate to simple wires. Then the problem is the discrete circuit shown in Fig. 33. Defining the transfer function H by

$$V_{out} = H\, V_{in} \qquad (10\text{-}3)$$

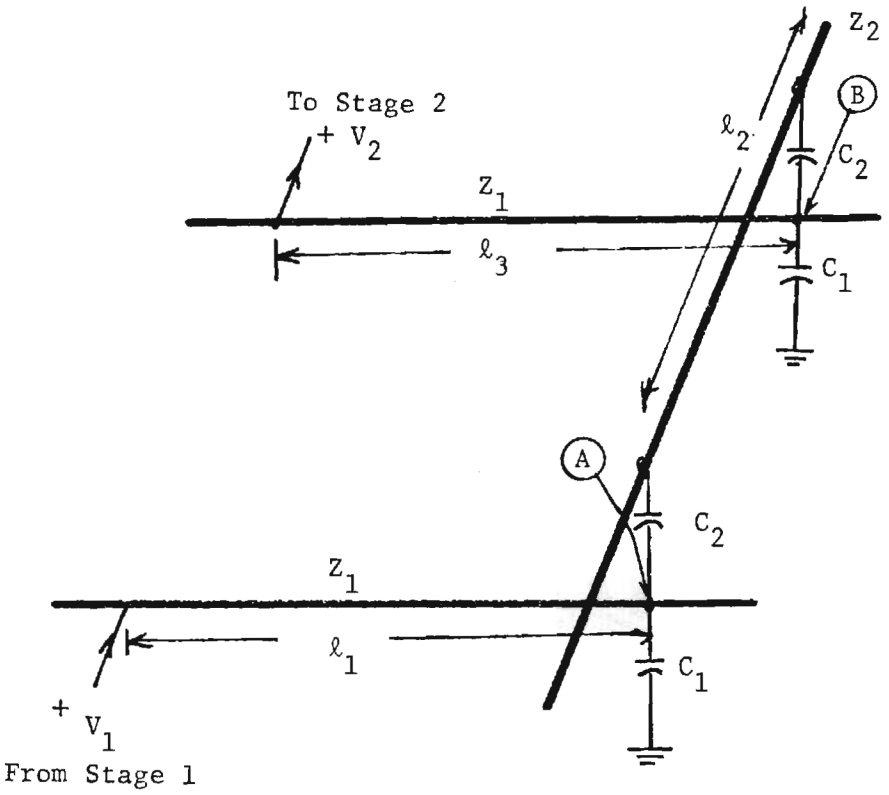


Figure 32

Transmission Line Model

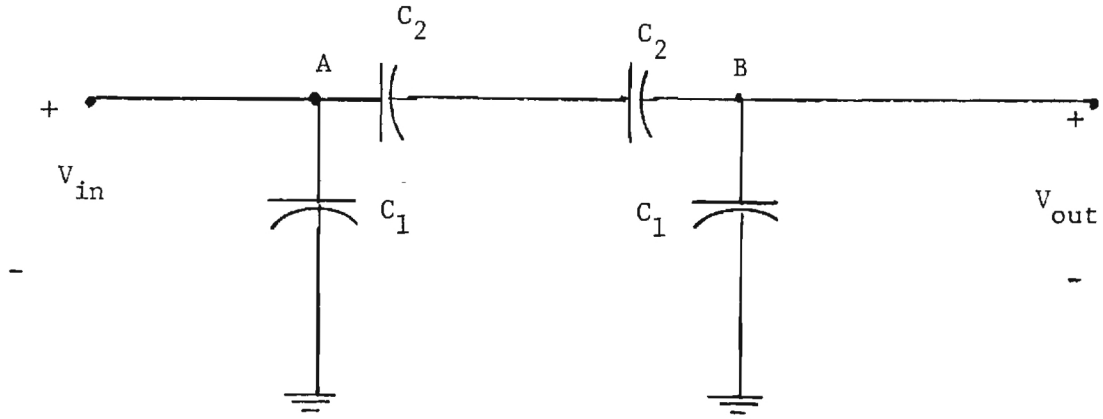


Figure 33

Long-Wavelength Lumped
Element Circuit

it is easily seen that

$$H = \frac{C_2}{C_2 + 2C_1} = \frac{d_1}{d_1 + 2d_2} \quad . \qquad (10\text{-}4)$$

Obviously, the interaction will be minimized by keeping $d_2 >> d_1$, which is equivalent to requiring that $C_1' >> C_2'$. This is understood on a physical basis by noting that this will minimize the coupling parasitic between the two lines. This simple solutions is what would be expected by basic reasoning.

The short-wavelength problem is a bit more complicated. Figure 34 shows the equivalent circuit used to compute the transfer function when transmission line effects must be included. The overlap between layer 1 and layer 2 is described by the coupling capacitance

$$C_2 = \frac{\varepsilon_{ox} w_1 w_2}{d_2} \qquad (10\text{-}5)$$

which ignores fringing fields. Two extra nodes marked "W" and "X" have been included to make the circuit calculation easier. Note that the characteristic line impedances are respectively denoted as Z_1 and Z_2.

The analysis is straightforward, but somewhat messy. Consequently, only the results will be presented here. The analysis allows for a transmission line equivalent circuit using the port representation illustrated in Fig. 35. The transfer functions are found to be

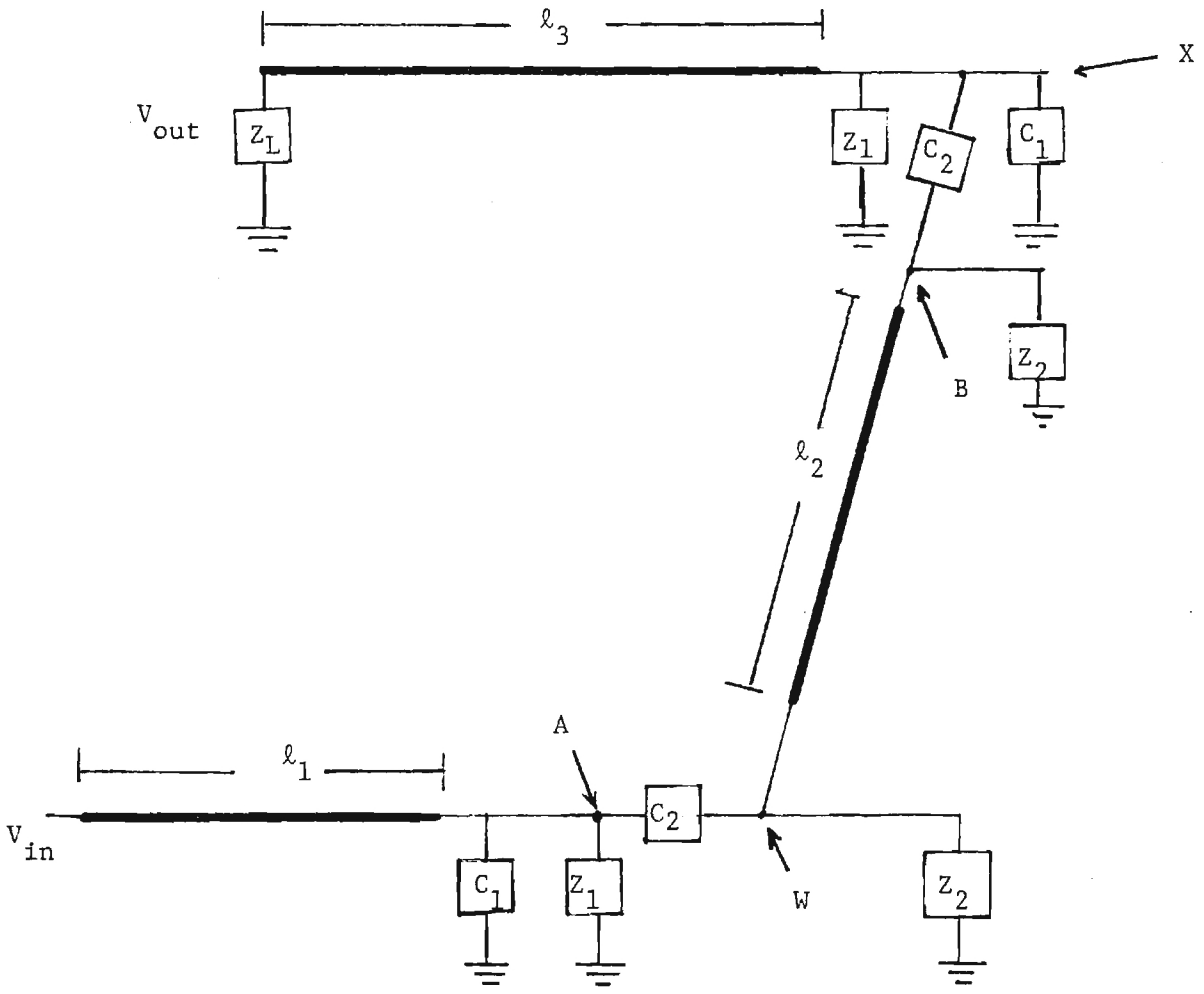


Figure 34

Equivalent Circuit for
Transmission Line
Calculation

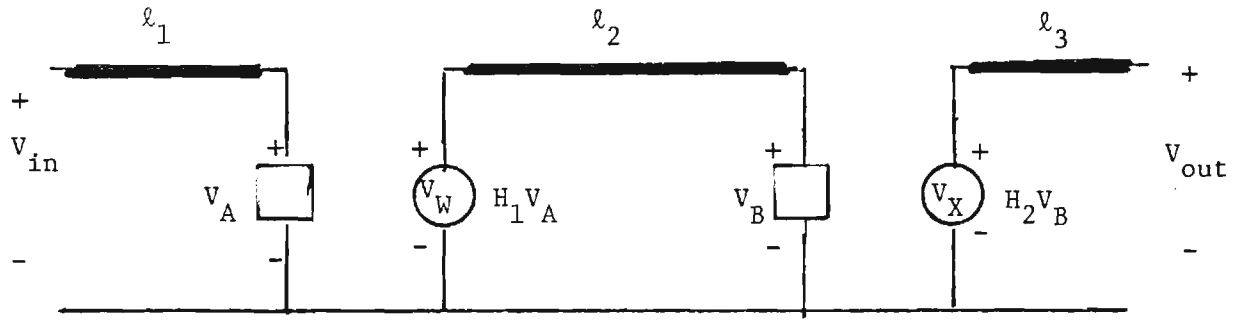


Figure 35

Simplified Port Representation

$$H_1 = \frac{Z_2 || Z_W}{Z_2 || Z_W + Z_{C2}}$$

$$H_2 = \frac{Z_1 || Z_{C1} || Z_X}{Z_1 || Z_{C1} || Z_x + Z_{C2}} \qquad (10\text{-}6)$$

where

$$Z_X = Z_1 \frac{Z_L + jZ_1 \tan(\beta \ell_3)}{Z_1 + jZ_L \tan(\beta \ell_3)} \qquad (10\text{-}7)$$

and

$$Z_W = Z_2 \frac{Z_z + jZ_2 \tan(\beta \ell_2)}{Z_2 + jZ_z \tan(\beta \ell_2)} \quad . \qquad (10\text{-}8)$$

The impedance Z_z is given by

$$Z_z = Z_2 || (Z_{C2} + Z_1 || Z_{C1} || Z_X) \qquad (10\text{-}9)$$

while

$$\beta = \frac{2\pi}{\lambda} \qquad (10\text{-}10)$$

is the wavenumber. The input impedance looking into the input port is found to be

$$Z_{in} = Z_1 \frac{Z_u + jZ_1 \tan(\beta \ell_1)}{Z_1 + jZ_u \tan(\beta \ell_1)} \qquad (10\text{-}11)$$

where

$$Z_u = Z_{C1}||Z_1||(Z_{C2} + Z_2||Z_W) \quad , \qquad (10\text{-}12)$$

Although these results seem somewhat complicated, they are easily understood by referring to the equivalent port network. The basic conclusion of the work was as expected, namely, the coupling will not be a problem so long as the lumped-parameter condition that $d_2 >> d_1$ is satisfied. It was intially anticipated that the coupling function could be important in creating a "radius of interference" about the origin of the input signal. However, two computer runs were sufficient to demonstrate that this type of problem will probably not exist in a realistic chip environment at current 4-5 micron dimensions. It is thought that this type of interaction will become crucially important in high density bipolar memories; however, such a study was beyond the scope of the research possible in the given time frame.

It should be mentioned that the study of intrinsic noise sources, such as shot and thermal noise voltages, was also studied for a short time during the project. The work was inconclusive as it was abandoned after the first runs indicated that the VTC would not be significantly changed from these extra sources.

11. Conclusions

The research described here has shown that the basic mechanism of VTC critical voltages in an ECL digital integrated circuit can be described by isolating the important dependences. The most influential factors in establishing the noise margins are the variations in the saturation current and the exact shape of the transfer curve used to model the transistors.

This work should be viewed as a starting point for future studies in this area. Although important questions have been answered, there are many remaining questions which need to be answered. In addition, the results should be applied to a specific process in order to obtain design criteria.

12. References

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